GigaDevice Semiconductor Inc.

GD33AP2361_AP2362_AP2363
System Base Chip

Datasheet

Revision 1.0

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Features

- **Dual LDO Regulators:** 5 V / 250 mA (optional 3.3 V) main and 5 V / 100 mA auxiliary with off-board protection.
- **External Regulation:** Supports external PNP for 5 V/3.3 V or 3.3 V/1.8 V extension.
- **CAN FD Transceiver:** ISO 11898-2:2016 & SAE J2284 compliant, up to 5 Mbit/s, with Partial Networking and FD-tolerant mode.
- **LIN Communication:** Up to two LIN 2.2 / ISO 17987-4 / SAE J2602 channels.
- **High-Side Outputs:** Four drivers (typ. 7 Ω), two HV GPIOs, three wake inputs.
- **Safety Functions:** Integrated watchdog, fail-safe logic, reset and interrupt outputs.
- **SPI Interface:** 16-bit SPI for configuration and diagnostics.
- **Automotive Grade:** AEC-Q100 Grade 1 qualified.

Applications

- Body Control Module (BCM)
- Keyless Entry and Start System
- Gateway Controller
- HVAC System
- Seat, Roof, Tailgate, Trailer and Door Module
- Lighting and Signal Control
- Gear Selector Interface

Description

The device is a Body System Integrated Circuit (IC) combining voltage regulation, power management, and in-vehicle communication functions in a single compact solution. It features dual low-dropout regulators, a high-speed CAN FD transceiver with Partial Networking support, and up to two LIN transceivers for distributed body electronics. Multiple high-side switches and high-voltage wake inputs enable flexible load control and system activation under demanding automotive conditions. With integrated safety supervision, diagnostic capability, and AEC - Q100 Grade 1 qualification, the device is ideal for next-generation automotive body control applications.

Product Variant	VCC1	VCC2	VCC3	CAN	CAN SWK	LIN
GD33AP2361F5AQC3TR	5V	5V	5V or 3.3V selectable	1	√	0
GD33AP2361U5AQC3TR	5V	5V	5V or 3.3V selectable	1	×	0
GD33AP2361F3AQC3TR	3.3V	5V	3.3V or 1.8V selectable	1	√	0
GD33AP2361U3AQC3TR	3.3V	5V	3.3V or 1.8V selectable	1	×	0
GD33AP2362F5AQC3TR	5V	5V	5V or 3.3V selectable	1	√	1
GD33AP2362U5AQC3TR	5V	5V	5V or 3.3V selectable	1	×	1
GD33AP2362F3AQC3TR	3.3V	5V	3.3V or 1.8V selectable	1	√	1
GD33AP2362U3AQC3TR	3.3V	5V	3.3V or 1.8V selectable	1	×	1

GD33AP2363F5AQC3TR	5V	5V	5V or 3.3V selectable	1	√	2
GD33AP2363U5AQC3TR	5V	5V	5V or 3.3V selectable	1	×	2
GD33AP2363F3AQC3TR	3.3V	5V	3.3V or 1.8V selectable	1	√	2
GD33AP2363U3AQC3TR	3.3V	5V	3.3V or 1.8V selectable	1	×	2

1 Overview

Scalable System Basis Chip Family

- Scalable product family designed to cover a wide range of automotive applications
- Full hardware and software compatibility across all variants
- GD33AP2363: 2 LIN transceivers, 1 CAN transceiver, 3 voltage regulators
- GD33AP2362: 1 LIN transceiver, 1 CAN transceiver, 3 voltage regulators
- GD33AP2361: No LIN transceiver, 1 CAN transceiver, 3 voltage regulators
- Variants available for 5 V (GD33AP236xx5) and 3.3 V (GD33AP236xx3) main regulator output
- CAN Partial Networking versions: 5 V (GD33AP236xF5) and 3.3 V (GD33AP236xF3)

Device Description

The GD33AP236x is a monolithic System Basis Chip (SBC) in an exposed-pad VQFN-48 (7 mm × 7 mm) package with Lead Tip Inspection (LTI) for Automatic Optical Inspection (AOI).

Designed for CAN-LIN automotive applications, it provides the main power supply for the microcontroller and acts as an interface for CAN and LIN networks, supporting CAN FD and Partial Networking.

The device integrates three low-dropout regulators (LDOs): a main 5 V regulator for MCU supply, a secondary 5 V LDO with off-board protection for sensors, and an external PNP driver regulator for off-board or load-sharing operation. It also includes a high-speed CAN FD transceiver with FD-tolerant mode, optional LIN transceivers, high-side switches with protection, and a 16-bit SPI interface for configuration and diagnostics.

Comprehensive supervision features include a configurable window watchdog, three fail outputs, and an undervoltage reset. The device supports low-power modes with wake-up via bus message, monitoring inputs, or cyclic wake, ensuring minimal current consumption in battery-connected systems.

Robustly designed for automotive environments, the GD33AP236x family delivers a scalable, reliable, and efficient solution for next-generation vehicle body electronics.

Product Features

- Very low quiescent current consumption in Stop and Sleep modes
- Periodic Cyclic Wake function in SBC Normal and Stop modes
- Periodic Cyclic Sense function available in SBC Normal, Stop, and Sleep modes
- Low-dropout voltage regulators (LDOs):
  - 5 V / 250 mA main regulator for MCU supply
  - 5 V / 100 mA secondary regulator with protection for off-board usage
  - External PNP driver regulator for load-sharing or stand-alone operation, current-limited by external shunt resistor (up to 350 mA with 470 mΩ resistor)
- High-speed CAN transceiver:
  - Fully compliant with ISO 11898-2:2016 (HS-CAN standard)
  - Supports CAN FD communication up to 5 Mbps
  - Compliant with CAN Partial Networking and FD-tolerant mode
- LIN transceivers: 0 to 2 channels (ISO 17987-4 / LIN 2.2 / SAE J2602) with configurable TXD timeout and LIN Flash Mode
- Four high-side switch outputs (typ. 7 Ω) with dedicated supply pin
- Two general-purpose high-voltage I/Os (GPIOs) configurable as Fail Outputs, Wake Inputs, Low-Side or High-Side switches

- Three universal high-voltage wake inputs for voltage level monitoring
- Alternate high-voltage measurement function, e.g. for battery voltage sensing
- Configurable wake-up sources via bus or I/O events
- Reset output and configurable timeout / window watchdog
- Up to three Fail Outputs (depending on configuration)
- Protection features: over-temperature and short-circuit protection
- Wide supply voltage and temperature range for automotive applications
- Green Product (RoHS compliant) and AEC-Q100 qualified
- VQFN-48 leadless exposed-pad package with Lead Tip Inspection (LTI) for Automatic Optical Inspection (AOI)

2 Block Diagram

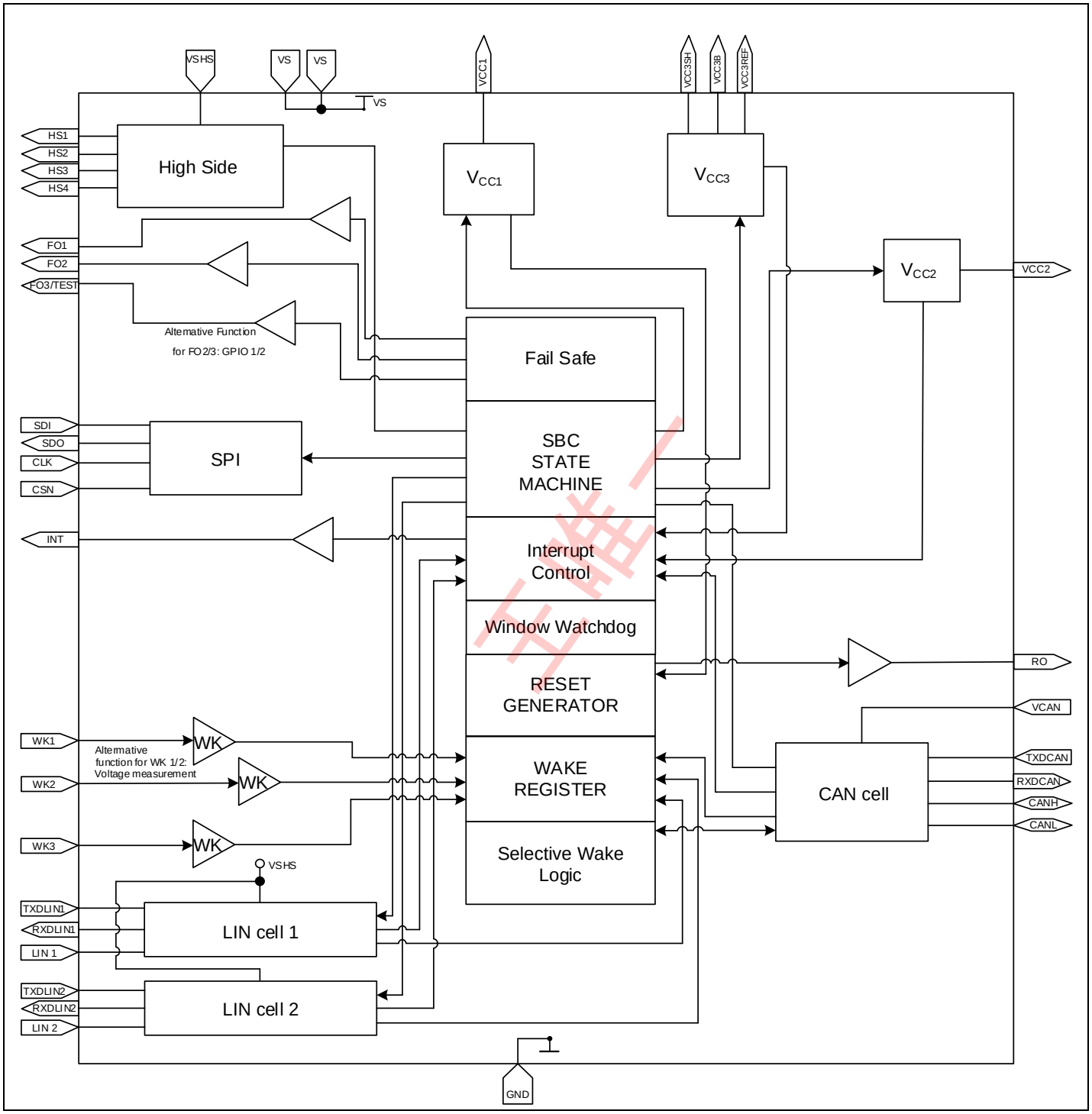


Figure 1 Block Diagram with CAN Partial Networking

Note:
For GD33AP2363 all the functions in the block diagram are available.
For GD33AP2362 LIN cell 2 (LIN2/TXDLIN2/RXDLIN2) is not available.
For GD33AP2361 LIN cell 1 and LIN cell 2 (LIN1/TXDLIN1/RXDLIN1/LIN2/TXDLIN2/RXDLIN2) are not available.

3 Pin Configuration

3.1 Pin Assignment

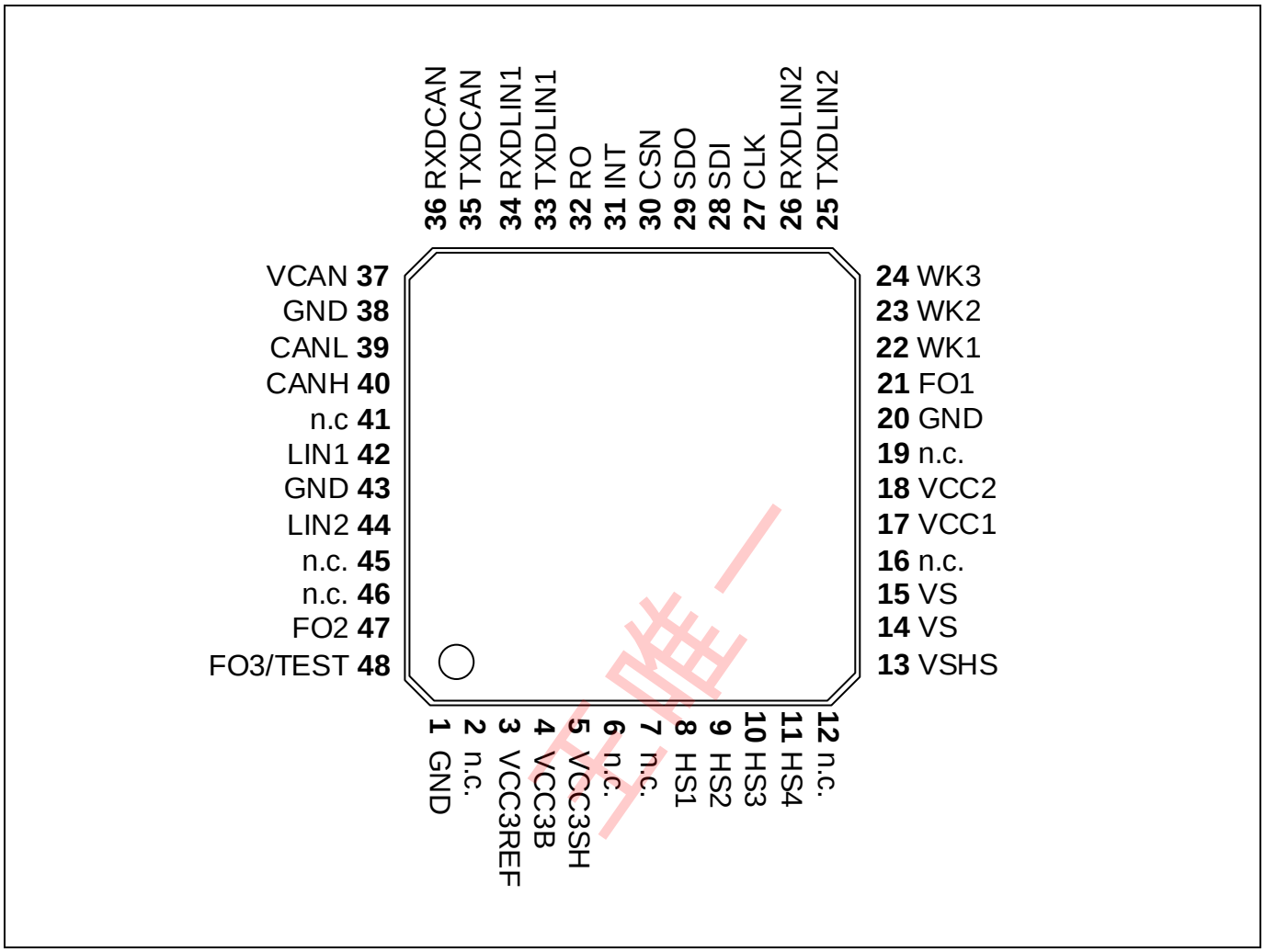


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	GND	**Ground**
2	n.c.	**not connected;** internally not bonded.
3	VCC3REF	**VCC3REF;** Collector connection for external PNP, reference input
4	VCC3B	**VCC3B;** Base connection for external PNP
5	VCC3SH	**VCC3SH;** Emitter connection for external PNP, shunt connection
6	n.c.	**not connected;** internally not bonded.
7	n.c.	**not connected;** internally not bonded.
8	HS1	**High Side Output 1;** typ. 7Ω
9	HS2	**High Side Output 2;** typ. 7Ω
10	HS3	**High Side Output 3;** typ. 7Ω
11	HS4	**High Side Output 4;** typ. 7Ω
12	n.c	**not connected;** internally not bonded.

Pin	Symbol	Function
13	VSHS	**Supply Voltage** for High-Side Switches and LIN and GPIO 1/2 in HS configuration; Connected to battery voltage with reverse protection diode and filter against EMC; Connect to VS if separate supply is not needed
14	VS	**Supply Voltage** for chip internal supply and voltage regulators; Connected to Battery Voltage with external reverse protection Diode and Filter against EMC
15	VS	**Supply Voltage** for chip internal supply and voltage regulators; Connected to Battery Voltage with external reverse protection Diode and Filter against EMC
16	n.c.	**not connected;** internally not bonded.
17	VCC1	**Voltage Regulator Output 1**
18	VCC2	**Voltage Regulator Output 2**
19	n.c.	**not connected;** internally not bonded.
20	GND	**Ground**
21	FO1	**Fail Output 1**
22	WK1	**Wake Input 1;** Alternative function: HV-measurement function input pin (only in combination with WK2, see **Chapter 12.2.2**)
23	WK2	**Wake Input 2;** Alternative function: HV-measurement function output pin (only in combination with WK1, see **Chapter 12.2.2**)
24	WK3	**Wake Input 3**
25	TXDLIN2	**Transmit LIN2 (for GD33AP2363)** Not used for GD33AP2362/ GD33AP2361 - Do not connect, leave open.
26	RXDLIN2	**Receive LIN2 (for GD33AP2363)** Not used for GD33AP2362/ GD33AP2361 - Do not connect, leave open.
27	CLK	**SPI Clock Input**
28	SDI	**SPI Data Input;** into SBC (=MOSI)
29	SDO	**SPI Data Output;** out of SBC (=MISO)
30	CSN	**SPI Chip Select Not Input**
31	INT	**Interrupt Output**; used as wake-up flag for microcontroller in SBC Stop or Normal Mode and for indicating failures. Active low. During start-up used to set the SBC configuration. External pull-up sets config 1/3, no external pull-up sets config 2/4.
32	RO	**Reset Output**
33	TXDLIN1	**Transmit LIN1 (for GD33AP2363/ GD33AP2362)** Not used for GD33AP2361 - Do not connect, leave open.
34	RXDLIN1	**Receive LIN1 (for GD33AP2363/GD33AP2362)** Not used for GD33AP2361 - Do not connect, leave open.
35	TXDCAN	**Transmit CAN**; alternate function: calibration of high-precision oscillator
36	RXDCAN	**Receive CAN**
37	VCAN	**Supply Input; for internal HS-CAN cell**
38	GND	**Ground**
39	CANL	**CAN Low Bus Pin**
40	CANH	**CAN High Bus Pin**
41	n.c.	**not connected;** internally not bonded.
42	LIN1	**LIN1 Bus (for GD33AP2363/GD33AP2362)** Not used for GD33AP2361 - Do not connect, leave open.

Pin	Symbol	Function
43	GND	**Ground**
44	LIN2	**LIN2 Bus (for GD33AP2363)** Not used for GD33AP2362/GD33AP2361 - Do not connect, leave open.
45	n.c.	**not connected;** internally not bonded.
46	n.c.	**not connected;** internally not bonded.
47	FO2	**Fail Output 2** - Side Indicator; Side indicators 1.25Hz 50% duty cycle output; Open drain. Active LOW. **Alternative Function: GPIO1**; configurable pin as WK, or LS, or HS supplied by VSHS (default is FO2, see also **Chapter 14.1.1**)
48	FO3/TEST	**Fail Output 3** - Pulsed Light Output; Break/rear light 100Hz 20% duty cycle output; Open drain. Active LOW **TEST**; Connect to GND to activate SBC Development Mode; Integrated pull-up resistor. Connect to VS with pull-up resistor or leave open for normal operation. **Alternative Function: GPIO2**; configurable pin as WK, or LS, or HS supplied by VSHS (default is FO3, see also **Chapter 14.1.1**)
Cooling Tab	GND	Cooling Tab - Exposed Die Pad; connect the exposed pad to GND. It is recommended to connect the exposed pad to a heat sink.

Note: All VS Pins must be connected to battery potential or insert a reverse polarity diodes where required; all GND pins as well as the Cooling Tab must be connected to one common GND potential; note that the tie bars at each package corner are connected to the cooling tab (see also **Chapter 18**)

3.3 Hints for Unused Pins

To ensure proper device operation, the correct configuration must be selected. Functions that are not used shall be disabled via SPI and pins treated as described below:

- WK1 / WK2 / WK3: Connect to GND and disable the wake inputs via SPI.
- HSx: Leave open.
- LINx, RXDLINx, TXDLINx, CANH, CANL, RXDCAN, TXDCAN: Leave all pins open.
- RO / FOx: Leave open.
- INT: Leave open.
- TEST: Connect to GND during power-up to activate the SBC Development Mode; connect to VS or leave open for normal user mode operation.
- VCC2: Leave open and keep disabled.
- VCC3: Refer to Chapter 8.5 for specific configuration details.
- VCAN: Connect to VCC1.
- n.c.: Not connected; internally not bonded; connect to GND.

If unused pins are routed to an external connector that leaves the ECU, provisions should be made for a zero ohm jumper (depopulated if unused) or appropriate ESD protection components.

3.4 Hints for Alternate Pin Functions

For pins with alternate functions selectable via SPI, it must be ensured that the correct configuration is properly set via SPI, especially in cases where it is not automatically configured. Please refer to the corresponding functional chapters for detailed descriptions.

In addition, the following considerations apply:

- WK1 / WK2:

These pins can be configured either as high-voltage wake or voltage monitoring inputs, or as voltage measurement inputs ((controlled by bit **WK_MEAS**). When used for voltage measurement, WK1 and WK2 shall not be assigned to any wake detection or cyclic sense functionality. WK1 and WK2 must be disabled in the register **WK_CTRL_2** and their level information should be ignored in registe **WK_LVL_STAT**.

- FO2 / FO3:
- These pins can alternatively be configured as GPIOs via the **GPIO_CTRL** register. When configured as GPIOs, they must not be used for any fail-output functionality. The default function after Power-on Reset (POR) is Fail Output (FOx).

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings[1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			
Voltages							
Supply Voltage (VS, VSHS)	$VS_{x, max}$	-0.3	–	28	V	–	
Supply Voltage (VS, VSHS)	$VS_{x, max}$	-0.3	–	40	V	Load Dump, max. 400 ms	
Voltage Regulator 1	$V_{CC1, max}$	-0.3	–	5.5	V	V_{CC1} = 5.6V for max. 10s	
Voltage Regulator 2	$V_{CC2, max}$	-0.3	–	28	V	V_{CC2} = 40V for Load Dump, max. 400 ms;	
Voltage Regulator 3 (VCC3REF)	$V_{CC3REF,max}$	-0.3	–	28	V	V_{CC3REF} = 40V for Load Dump, max. 400 ms;	
Voltage Regulator 3 (VCC3B)	$V_{CC3B,max}$	-0.3	–	V_S + 10	V	V_{CC3B} = 40V for Load Dump, max. 400 ms;	
Voltage Regulator 3 (VCC3SH)	$V_{CC3SH,max}$	V_S - 0.30	–	V_S + 0.30	V	–	
Wake Inputs WK1..3	$V_{WK, max}$	-0.3	–	40	V	–	
Fail Pin FO1	$V_{FO1, max}$	-0.3	–	40	V	–	
Fail Pins FO2, FO3/TEST	$V_{FO2\_3, max}$	-0.3	–	V_S + 0.3	V	–	
LINx, CANH, CANL	$V_{BUS, max}$	-27	–	40	V	–	
Maximum Differential CAN Bus Voltage	$V_{CAN\_Diff, max}$	-40	–	40	V	–	
Logic Input Pins (CSN, CLK, SDI, TXDLINx, TXDCAN)	$V_{I, max}$	-0.3	–	V_{CC1} + 0.3	V	–	
Logic Output Pins (SDO, RO, INT, RXDLINx, RXDCAN)	$V_{O, max}$	-0.3	–	V_{CC1} + 0.3	V	–	
VCAN Input Voltage	$V_{VCAN, max}$	-0.3	–	5.5	V	–	
High Side 1...4	$V_{HS, max}$	-0.3	–	V_{SHS} + 0.3	V	–	
Currents							
Wake input WK1	$I_{WK1,max}$	0	–	500	µA	2)	

Table 1 Absolute Maximum Ratings[1] (cont'd)

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			
Wake input WK2	$I_{WK2,max}$	-500	_	0	µA	[2]	
Temperatures							
Junction Temperature	T_j	-40	_	150	°C	_	
Storage Temperature	T_{stg}	-55	_	150	°C	_	
ESD Susceptibility							
ESD Resistivity	$V_{ESD,11}$	-2	_	2	kV	HBM[3]	
ESD Resistivity to GND, HSx	$V_{ESD,12}$	-2	_	2	kV	HBM[3]	
ESD Resistivity to GND, CANH,CANL, LINx	$V_{ESD,13}$	-8	_	8	kV	HBM[4][3]	
ESD Resistivity to GND	$V_{ESD,21}$	-500	_	500	V	CDM[5]	
ESD Resistivity Pin 1, 12,13,24,25,36,37,48 (corner pins) to GND	$V_{ESD,22}$	-750	_	750	V	CDM[5]	

1) Not subject to production test, specified by design
2) Applies only if WK1 and WK2 are configured as alternative HV-measurement function
3) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS-001 (1.5kΩ, 100pF)
4) For ESD "GUN" Resistivity 6KV (according to IEC61000-4-2 "gun test" (150pF, 330Ω)), will be shown in Application Information.
5) ESD susceptibility, Charged Device Model according to ANSI/ESDA/JEDEC JS-002

Notes

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Table 2 Functional Range

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			
Supply Voltage	$V_{S,func}$	V_{POR}	_	28	V	[1] V_{POR} see **Chapter 15.10**	
LIN Bus Voltage	$V_{S,LIN,func}$	6	_	18	V	[2]	
CAN Supply Voltage	$V_{CAN,func}$	4.75	_	5.25	V	_	
SPI frequency	f_{SPI}	–	_	4	MHz	see **Chapter 16.7** for $f_{SPI,max}$	
Junction Temperature	T_j	-40	_	150	°C	_	

1) Including Power-On Reset, Over- and Undervoltage Protection
2) Parameter Specification according to LIN 2.2/ISO 17987-4

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

Functional Behavior in Extended Voltage Conditions:

- 28 V < VS,func < 40 V:
  The device, including its internal state machine, remains functional. Regulators VCC1/2/3 operate normally, but thermal shutdown may occur due to excessive power dissipation. HSx switches may turn OFF depending on VSHS_OV configuration. SPI communication speed remains within specification. Although absolute maximum ratings are not violated, the device is not intended for continuous operation above 28 V. Extended operation at high junction temperatures may reduce operating lifetime.

- 18V < $V_{S,LIN}$ <28V:
  The LIN transceiver remains functional, but communication reliability may be degraded due to operation outside LIN specification.

- $V_{SHS,UVD}$ < $V_{S,LIN}$ < 6V:
  The LIN transceiver remains functional; however, communication may fail under out-of-spec conditions.

- V_{CAN} < 4.75V:
  The undervoltage bit **VCAN_UV** is set in SPI register **BUS_STAT_1.** The CAN transmitter is **disabled** while the undervoltage condition persists

- 5.25V < V_{CAN} < 5.50V:
  The CAN transceiver remains functional, but communication quality may be affected due to out-of-spec operation.

- $V_{POR,f}$< VS < 5.5V:
  The device remains functional, though specified electrical parameters may no longer be ensured. The following behaviors apply under these conditions:
  – Voltage regulators enter low-drop operation mode (applies for VCC3 only if bit **VCC3_VS_ UV_OFF** is set).
  – A VCC1_UV reset may be triggered depending on Vrtx settings.
  – The LIN transmitter is disabled once $V_{SHS,UVD}$ threshold is reached.
  – HSx switch behavior depends on configuration:
  - **HS_UV_SD_EN** = '0' (default): HSx will be turned OFF for VSHS < VSHS_UV and will stay OFF.
  - **HS_UV_SD_EN** = '1': HSx stays ON as long as possible; an unwanted over-current shutdown may occur, setting the OC shutdown bit and keeping HSx OFF.
  – FOx outputs remain ON if previously enabled before VS > 5.5 V.
  – The SPI communication speed remains within specification.

4.3 Thermal Resistance

Table 3 Thermal Resistance[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			
Junction to Soldering Point	R_{thJSP}	–	6	–	K/W	Exposed Pad	
Junction to Ambient	R_{thJA}	–	33	–	K/W	2)	

1) Not subject to production test, specified by design.
2) According to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board for 1.5W.Board: 76.2x114.3x1.5mm^3 with 2 inner copper layers (35µm thick), with thermal via array under the exposed pad contacting the first inner copper layer and 300mm^2 cooling area on the bottom layer (70µm).

4.4 Current Consumption

Table 4 Current Consumption

Current consumption values are specified at T_j = 25°C, V_S = 13.5V, all outputs open (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			
SBC Normal Mode							
Normal Mode current consumption	I_{Normal}	–	0.1	1	mA	V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; VCC2, CAN,LIN,VCC3, HSx = OFF	
SBC Stop Mode							
Stop Mode current consumption	$I_{Stop\_1,25}$	–	80	–	µA	1)VCC2/3, HSx = OFF; CAN2), LINx,WKx not wake capable; Watchdog = OFF; no load on VCC1; **I_PEAK_TH** = '0'	
Stop Mode current consumption	$I_{Stop\_1,85}$	–	–	120	µA	1)3)T_j = 85°C; VCC2/3, HSx = OFF; CAN2), LINx,WKx not wake capable; Watchdog = OFF; no load on VCC1; **I_PEAK_TH** = '0'	
Stop Mode current consumption (high active peak threshold)	$I_{Stop\_2,25}$	–	80	–	µA	1)VCC2/3, HSx = OFF; CAN2), LINx,WKx not wake capable; Watchdog = OFF; no load on VCC1; **I_PEAK_TH** = '1'	
Stop Mode current consumption (high active peak threshold)	$I_{Stop\_2,85}$	–	–	120	µA	1)3)T_j = 85°C; VCC2/3, HSx = OFF; CAN2), LINx,WKx not wake capable; Watchdog = OFF; no load on VCC1; **I_PEAK_TH** = '1'	
SBC Sleep Mode							
Sleep Mode current consumption	$I_{Sleep,25}$	–	28	–	µA	VCC2/3, HSx = OFF; CAN2), LINx,WKx not wake capable	
Sleep Mode current consumption	$I_{Sleep,85}$	–	–	45	µA	3)T_j = 85°C; VCC2/3, HSx = OFF; CAN2), LINx,WKx not wake capable	

Table 4 Current Consumption (cont'd)

Current consumption values are specified at T_j = 25°C, V_S = 13.5V, all outputs open (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			
Feature Incremental Current Consumption							
Current consumption for CAN module, recessive state	$I_{CAN,rec}$	–	2	3	mA	SBC Normal/Stop Mode; CAN Normal Mode; VCC1 connected to VCAN; VTXDCAN =VCC1; no RL on CAN	
Current consumption for CAN module, dominant state	$I_{CAN,dom}$	–	3	4.5	mA	3)SBC Normal/Stop Mode; CAN Normal Mode; VCC1 connected to VCAN; VTXDCAN = GND; no RL on CAN	
Current consumption for CAN module, Receive Only Mode	$I_{CAN,RcvOnly}$	–	0.9	1.2	mA	3)4)SBC Normal/Stop Mode; CAN Receive Only Mode; VCC1 connected to VCAN; VTXDCAN = VCC1; no RL on CAN	
Current consumption during CAN Partial Networking frame detect mode (**RX_WK_ SEL** = '0')	$I_{CAN,SWK,25}$	–	560	690	µA	3)T_j = 25°C; SBC Stop Mode; VCC2, HSx = OFF; LIN,WKx not wake capable; CAN SWK wake capable, SWK Receiver enabled, WUF detect; no RL on CAN	
Current consumption during CAN Partial Networking frame detect mode (**RX_WK_ SEL** = '0')	$I_{CAN,SWK,85}$	–	–	720	µA	3)T_j = 85°C; SBC Stop Mode; VCC2, HSx = OFF; LIN,WKx not wake capable; CAN SWK wake capable, SWK Receiver enabled, WUF detect; no RL on CAN	

Table 4 Current Consumption (cont'd)

Current consumption values are specified at T_j = 25°C, V_S = 13.5V, all outputs open (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			

Current consumption per LIN module, recessive state	$I_{LIN,rec}$	–	0.1	1	mA	SBC Normal/Stop Mode; LIN Normal Mode; VTXDLIN = VCC1; no RL on LIN	
Current consumption per LIN module, dominant state	$I_{LIN,dom}$	–	1.0	1.5	mA	3)SBC Normal/Stop Mode; LIN Normal Mode; VTXDLIN = GND; no RL on LIN	
Current consumption per LIN module, Receive Only Mode	$I_{LIN,RcvOnly}$	–	0.2	0.5	mA	3)SBC Normal/Stop Mode; LIN Receive Only Mode; VTXDLIN = VCC1; no RL on LIN	
Current consumption for WK1..3 wake capability (all wake inputs)	$I_{Wake,WKx,25}$	–	0.2	2	µA	5)6)7) SBC Sleep Mode; WK1..3 wake capable (all WKx enabled); LIN, CAN = OFF	
Current consumption for WK1..3 wake capability (all wake inputs)	$I_{Wake,WKx,85}$	–	0.5	3	µA	3)5)6)7)SBC Sleep Mode; T_j = 85°C; WK1..3 wake capable; (all WKx enabled); LIN, CAN = OFF	
Current consumption per LIN module wake capability	$I_{Wake,LIN,25}$	–	5	–	µA	5)SBC Sleep Mode; LIN wake capable; WK1..3, CAN = OFF	
Current consumption per LIN module wake capability	$I_{Wake,LIN,85}$	–	–	7	µA	3)5)SBC Sleep Mode; T_j = 85°C; LIN wake capable; WK1..3, CAN = OFF	
Current consumption for CAN wake capability (tsilence expired)	$I_{Wake,CAN,25}$	–	9	–	µA	2)5)SBC Sleep Mode; CAN wake capable; WK1..3, LIN = OFF	
Current consumption for CAN wake capability (tsilence expired)	$I_{Wake,CAN,85}$	–	–	15	µA	2)3)5)SBC Sleep Mode; T_j = 85°C; CAN wake capable; WK1..3, LIN = OFF	
VCC2 Normal Mode current consumption	$I_{Normal,VCC2}$	–	35	100	µA	V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; VCC2 = ON (no load)	

Table 4 Current Consumption (cont'd)

Current consumption values are specified at T_j = 25°C, V_S = 13.5V, all outputs open (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			

Current consumption for VCC2 in SBC Sleep Mode	$I_{Sleep,VCC2,25}$	–	33	–	µA	1)5)SBC Sleep Mode; VCC2 = ON (no load); LIN, CAN, WK1..3 = OFF	
Current consumption for VCC2 in SBC Sleep Mode	$I_{Sleep,VCC2,85}$	–	–	45	µA	1)3)5)SBC Sleep Mode; T_j = 85°C; VCC2 = ON (no load); LIN, CAN, WK1..3 = OFF	
Current consumption for VCC3 in SBC Sleep Mode in stand-alone configuration	$I_{Sleep,VCC3,25}$	–	70	–	µA	1)5)SBC Sleep Mode; VCC3 = ON (no load, stand-along config.); LIN, CAN, WK1..3 = OFF	
Current consumption for VCC3 in SBC Sleep Mode in stand-alone configuration	$I_{Sleep,VCC3,85}$	–	–	80	µA	1)3)5)SBC Sleep Mode; T_j = 85°C; VCC3 = ON (no load, stand-along config.); LIN, CAN, WK1..3 = OFF	
Current consumption for HSx in SBC Stop Mode	$I_{Stop,HSx,25}$	–	550	–	µA	5)8)SBC Stop Mode; Cyclic Sense & HSx= ON (no load); LIN, CAN, WK1..3 = OFF	
Current consumption for HSx in SBC Stop Mode	$I_{Stop,HSx,85}$	–	–	700	µA	3)5)8)SBC Stop Mode; T_j = 85°C; Cyclic Sense & HSx = ON (no load); LIN, CAN, WK1..3 = OFF	
Current consumption for cyclic sense function	$I_{Stop,CS25}$	–	29	–	µA	5)9)10)SBC Stop Mode; WD = OFF	
Current consumption for cyclic sense function	$I_{Stop,CS85}$	–	–	35	µA	3)5)9)10)SBC Stop Mode; T_j = 85°C; WD = OFF	
Current consumption for watchdog active in Stop Mode	$I_{Stop,WD25}$	–	5	–	µA	3)SBC Stop Mode; Watchdog running	
Current consumption for watchdog active in Stop Mode	$I_{Stop,WD85}$	–	–	35	µA	3)SBC Stop Mode; T_j = 85°C; Watchdog running	

Table 4 Current Consumption (cont'd)

Current consumption values are specified at T_j = 25°C, V_S = 13.5V, all outputs open (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			
Current consumption for active fail outputs (FO1..3)	$I_{Stop,FOx}$	–	0.4	2.0	mA	3)all SBC Modes; T_j = 25°C; FOx = ON (no load);	

Current consumption for GPIOx if configured as low-side/high-side for SBC Stop or Sleep mode	$I_{Stop,GPIOx,LS/HS}$	–	450	–	µA	3)SBC Stop/Sleep mode; GPIO configured as LS/HS (no load);	
Current consumption for GPIOx if configured as low-side/high-side for SBC Stop or Sleep mode	$I_{Stop,GPIOx,LS/HS}$	–	–	600	µA	3)SBC Stop/Sleep mode; Tj = -40…150°C; GPIO configured as LS/HS (no load);	

1) If the load current on VCC1 will exceed the configured VCC1 active peak threshold $I_{VCC1,Ipeak1,r}$ or $I_{VCC1,Ipeak2,r}$, the current consumption may increase slightly to ensure optimum dynamic load behavior. See also **Chapter 6**, **Chapter 7**, **Chapter 8**.
2) CAN not configured in selective wake mode.
3) Not subject to production test, specified by design.
4) Current consumption adder also applies for during WUF detection (frame detect mode) when CAN Partial Networking is activated.
5) Current consumption adders of features defined for SBC Sleep Mode also apply for SBC Stop Mode and vice versa (unless otherwise specified).
6) No pull-up or pull-down configuration selected.
7) The specified WKx current consumption adder for wake capability applies regardless how many WK inputs are activated.
8) A typ. 75µA adder applies for every additionally activated HSx switch in SBC Stop Mode; In SBC Normal Mode every HSx switch consumes the typ. 75 µA without the initial adder because the biasing is already enabled.
9) HS1 used for cyclic sense, Timer 2, 20ms period, 0.1ms on-time, no load on HS1.
In general the current consumption adder for cyclic sense in SBC Stop Mode can be calculated with below equation:
IStop,CS (typ.) = 29µA + (550µA *tON/TPer)
10) Also applies to Cyclic Wake

Note: There is no additional current consumption contribution due to PWM generators.

5 System Features

This chapter describes the system features and operational behavior of the GD33AP236x:

- State machine
- SBC mode control
- Device configuration
- Supply and peripheral status
- System functions such as cyclic sense and cyclic wake
- Supervision and diagnostic functions

Operating Modes

The SBC provides six main operating modes:

- SBC Init Mode:
  Activated during device power-up or after a soft reset.
- SBC Normal Mode:
  The main operating mode for standard system functionality.
- SBC Stop Mode:
  First-level power-saving mode with the main voltage regulator VCC1 enabled.
- SBC Sleep Mode:
  Second-level power-saving mode with VCC1 disabled to minimize current consumption.
- SBC Restart Mode:
  An intermediate mode entered after a wake event from SBC Sleep or Fail-Safe Mode, or after a system failure (e.g., watchdog trigger failure or VCC1 undervoltage reset).
  It brings the microcontroller into a defined reset state.
  Once the failure condition is cleared, the device automatically returns to SBC Normal Mode after a delay time (tRD1).
- SBC Fail-Safe Mode:
  A safe-state mode activated after critical failures (e.g., watchdog failure or VCC1 undervoltage reset), ensuring the system enters a stable and recoverable state.
  VCC1 is disabled, and the device remains in this mode until either a wake event (via CAN, LINx, or WKx) occurs or the over-temperature condition is cleared.

A special mode called SBC Development Mode is available for software development and debugging.All operating modes can be accessed in this mode; however, the watchdog counter is halted and does not require regular triggering. This mode is entered by setting the TEST pin to GND during SBC Init Mode.

The device can be configured via hardware (external components) to define behavior after a watchdog trigger failure. Further details are provided in **Chapter 5.1.1.**

The System Basis Chip is controlled via a 16-bit SPI interface. A detailed description can be found in **Chapter 16**.The configuration as well as the diagnosis is handled via the SPI.

5.1 Block Description of State Machine

The different SBC operating modes can be selected via SPI by setting the corresponding SBC **MODE** bits in the register **M_S_ CTRL**. When the device enters SBC Restart Mode, these bits are automatically cleared, ensuring that the register always reflects the current active SBC mode.

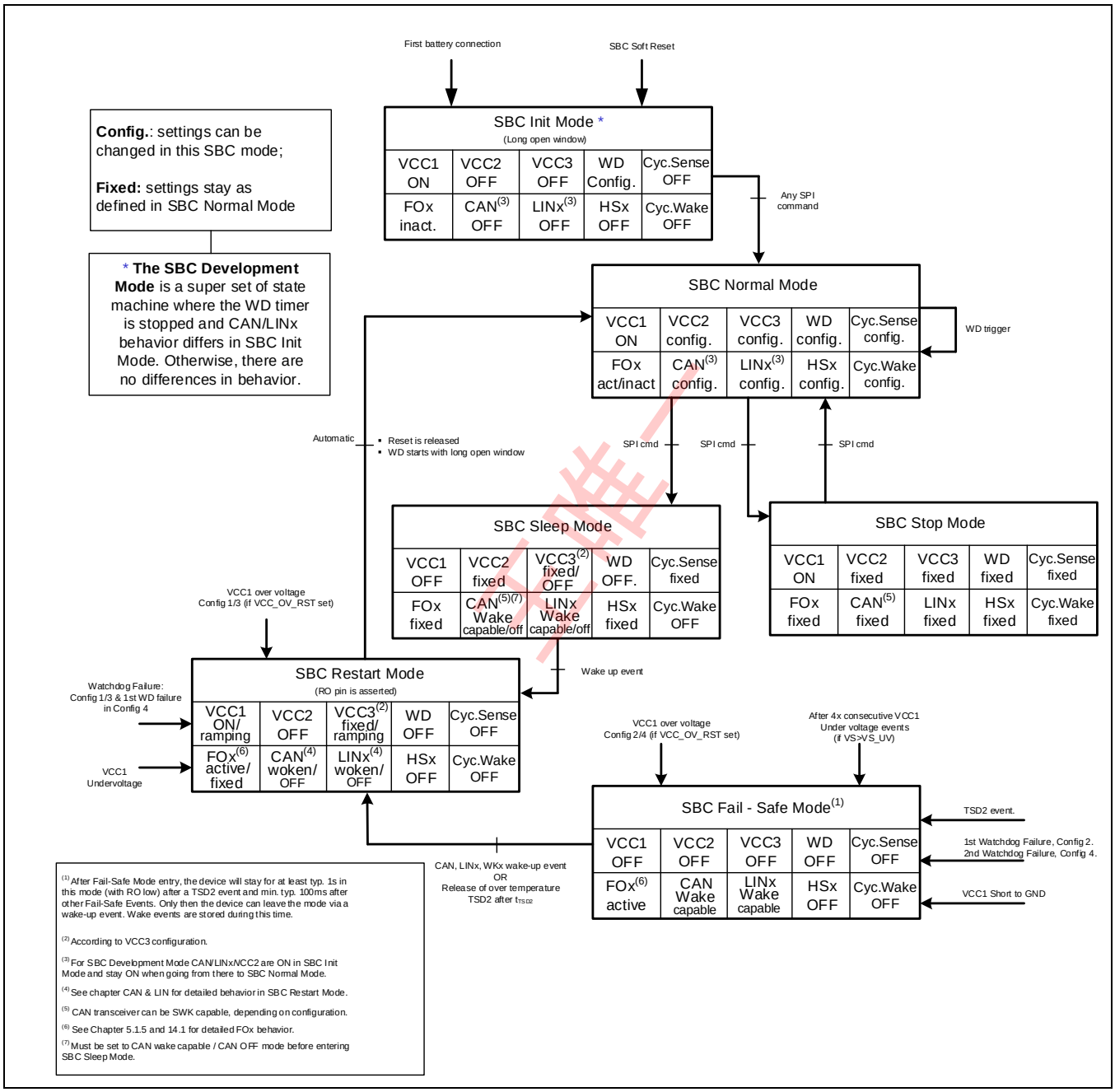


Figure 3 State Diagram showing the SBC Operating Modes including CAN Partial Networking

5.1.1 Device Configuration and SBC Init Mode

The SBC enters Init Mode after the supply voltage crosses the power-on reset threshold $V_{POR,r}$ (see also **Chapter 15.3**). At this stage, the watchdog is activated with a long open window (t_{LW})to allow proper system initialization.

During this power-on phase, the following configurations are latched into the device:

- The device behavior in response to a watchdog trigger failure and VCC1 overvoltage condition is determined by the external circuitry connected to the INT pin (see below).

- The operating mode selection either
  normal operation or SBC Development Mode (with watchdog disabled for debugging) is defined by the voltage level on the FO3/TEST pin (see also **Chapter 5.1.7**).

5.1.1.1 Device Configuration

The device configuration defines the SBC behavior in case of a watchdog trigger failure.Depending on the application requirements, the VCC1 output can either remain ON or be switched OFF when a watchdog failure occurs (after one or two missed triggers).To configure the device so that VCC1 is switched OFF and the SBC enters Fail - Safe Mode upon a watchdog failure (Config 2/4), the INT pin does not require an external pull-up resistor.If VCC1 should remain enabled after a watchdog failure (Config 1/3), the INT pin must be connected to VCC1 through an external pull-up resistor (see application diagram in **Chapter 17.1**).

Figure5 illustrates the timing of the hardware configuration selection.The hardware configuration is defined during SBC Init Mode.During the reset delay time (t_{RD1}), i.e., after VCC1 crosses the reset threshold (VRT1) and before the RO pin goes HIGH, the INT pin is internally pulled LOW by a weak pull-down resistor.The INT pin voltage is monitored during this period (with a continuous filter time t_{CFG_F}), and the configuration value — determined by the voltage level at INT — is latched at the rising edge of RO.

Note: If the **POR** bit is not cleared then the internal pull-down resistor will be reactivated every time RO is pulled LOW the configuration will be updated at the rising edge of RO. Therefore it is recommended to clear the **POR** bit right after initialization. In case there is no stable signal at INT, then the default value '0' will taken as the config select value = SBC Fail-Safe Mode.

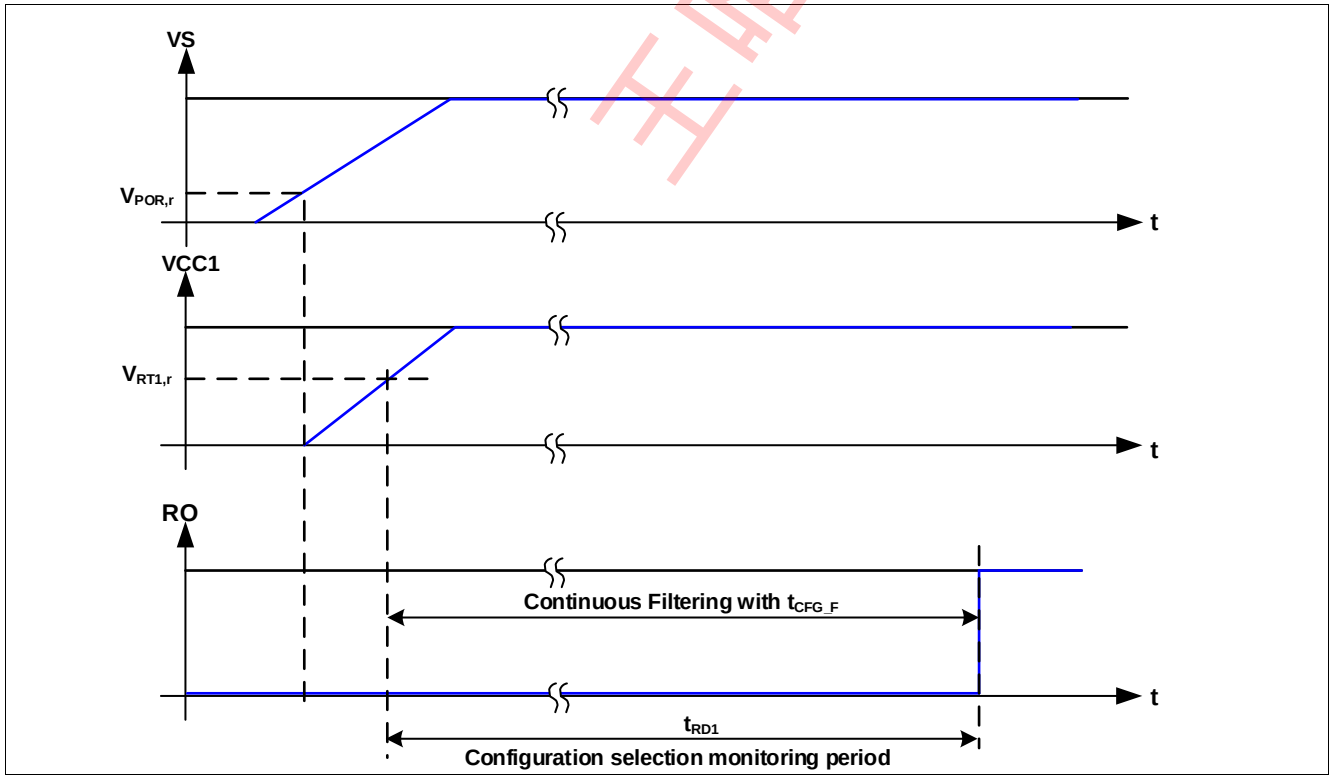


Figure 4 Hardware Configuration Selection Timing Diagram

There are four different device configurations (**Table 5**) available defining the watchdog failure and the VCC1 overvoltage behavior. The configurations can be selected via the external connection on the INT pin and the SPI bit **CFG** in the **HW_CTRL** register (see also **Chapter 16.4**):

- CFGP = '1': Config 1 and Config 3:
  1) A watchdog trigger failure leads to SBC Restart Mode and depending on CFG the Fail Outputs (FOx) are activated after the 1st (Config 1) or 2nd (Config 3) watchdog trigger failure;
  2) A VCC1 overvoltage detection will lead to SBC Restart Mode if **VCC1_OV_RST** is set. **VCC1_OV** will be set and the Fail Outputs are activated;

- CFGP = '0': Config 2 and Config 4:
  1) A watchdog trigger failure leads to SBC Fail-Safe Mode and depending on CFG the Fail Outputs (FOx) are activated after the 1st (Config 2) or 2nd (Config 4) watchdog trigger failure. The first watchdog trigger failure in Config 4 will lead to SBC Restart Mode;
  2) A VCC1 overvoltage detection will lead to SBC Fail-Safe Mode if **VCC1_OV_RST** is set. **VCC1_OV** will be set and the Fail Outputs are activated;

The respective device configuration can be identified by reading the SPI bit **CFG** in the **HW_CTRL** register and the **CFGP** bit in the **WK_LVL_STAT** register.

Table 5 shows the configurations and the device behavior in case of a watchdog trigger failure:

Table 5 Watchdog Trigger Failure Configuration

Config	INT Pin (CFGP)	SPI Bit CFG	RO activation	FOx activation	SBC Mode Entry
1	External pull-up	1	each watchdog failure	after 1st WD failure	SBC Restart Mode
2	No ext. pull-up	1	each watchdog failure	after 1st WD failure	SBC Fail-Safe Mode after 1st WD failure
3	External pull-up	0	each watchdog failure	after 2nd WD failure	SBC Restart Mode
4	No ext. pull-up	0	each watchdog failure	after 2nd WD failure	SBC restart mode after 1st WD failure. SBC Fail-Safe Mode after 2nd WD failure

Table 6 shows the configurations and the device behavior in case of a VCC1 overvoltage detection when **VCC1_OV_RST** is set:

Table 6 Device Behavior in Case of VCC1 Overvoltage Detection

Config	INT Pin (CFGP)	CFG Bit	VCC1_OV_RST	Event	VCC1_OV	FOx Activation	SBC Mode Entry
1-4	any value	x	0	1 x VCC1 OV	1	no FOx activation	unchanged
1	External pull-up	1	1	1 x VCC1 OV	1	after 1st VCC1 OV	SBC Restart Mode
2	No ext. pull-up	1	1	1 x VCC1 OV	1	after 1st VCC1 OV	SBC Fail-Safe Mode
3	External pull-up	0	1	1 x VCC1 OV	1	after 1st VCC1 OV	SBC Restart Mode
4	No ext. pull-up	0	1	1 x VCC1 OV	1	after 1st VCC1 OV	SBC Fail-Safe Mode

The respective configuration will be stored for all conditions and can only be changed by powering down the device (VS < $V_{POR,f}$).

5.1.1.2 SBC Init Mode

In SBC Init Mode, the device waits for the microcontroller to complete its startup and initialization sequence. During this mode, any valid SPI command will transition the SBC to SBC Normal Mode.Within the long open win dow (t_{LW}), the watchdog must be triggered once; doing so automatically configures the watchdog parameters.If n o watchdog trigger occurs during this interval, a watchdog failure is detected and the device enters SBC Restart Mode.

All wake-up events are ignored during SBC Init Mode and will therefore be lost.

Notes
1. Any SPI command will bring the SBC to Normal Mode, even if the command is illegal (see **Chapter 16.2**).
2. For a safe startup, it is recommended to use the first SPI command to trigger and configure the watchdog (se e **Chapter 15.2**).

3. During power-up, no **VCC1_UV**event will be issued, nor will any FOx signal be triggered as long as VCC1 re mains below the $V_{RT,x}$ threshold and VS is below the VCC1 short-circuit detection threshold **($V_{S,UV}$)**. The RO p in will remain LOW as long as VCC1 is below the selected $V_{RT,x}$ threshold.

5.1.2 SBC Normal Mode

The SBC Normal Mode represents the standard operating mode of the device. All configuration activities must be completed in this mode before transitioning into any low-power mode (see also **Chapter 5.1.6** for details on Fail-Safe Mode configuration).

A wake-up event on CAN, LINx, or WKx will generate an interrupt on the INT pin, but it will not change the current SBC mode.

- VCC1 is active
- VCC2 can be switched ON or OFF (default = OFF)
- VCC3 is configurable (OFF coming from SBC Init Mode; as previously programmed coming from SBC Restart Mode)
- CAN is configurable (OFF coming from SBC Init Mode; OFF or wake capable coming from SBC Restart Mode, see also **Chapter 5.1.5**)
- LIN is configurable (OFF coming from SBC Init Mode; OFF or wake capable coming from SBC Restart Mode, see also **Chapter 5.1.5**)
- HS Outputs can be switched ON or OFF (default = OFF) or can be controlled by PWM; HS Outputs are OFF coming from SBC Restart Mode
- Wake pins show the input level and can be selected to be wake capable (interrupt)
- Cyclic sense can be configured with HS1...4 and Timer1 or Timer2
- Cyclic wake can be configured with Timer1 or Timer2
- Watchdog is configurable
- All FOx outputs are OFF by default. Coming from SBC Restart Mode FOx can be active (due to a failure event, e.g. watchdog trigger failure,VCC1 short circuit, etc.) or inactive (no failure occurred)

In SBC Normal Mode, the FO outputs can be tested to verify the intended system response when the FO pin is dr iven LOW. The microcontroller can enable and disable the FO output by setting the **FO_ON** SPI bit.
This feature is provided for testing purposes only and should not be used during normal operation.

5.1.3 SBC Stop Mode

The SBC Stop Mode is the first-level low-power technique used to reduce the overall current consumption by placing the voltage regulators VCC1, VCC2, and VCC3 into a low-power state. In this mode, VCC1 remains active, continuing to supply the microcontroller, which may itself enter a power-down mode. The VCC2 supply, CAN and LIN interfaces, as well as the HSx outputs can be configured to remain enabled if required. All necessary configurations must be completed before entering SBC Stop Mode. Within SBC Stop Mode, any SPI WRITE command is ignored and the **SPI_FAIL** bit is set, except for the following operations: Transitioning to SBC Normal Mode, Triggering an SBC Soft Reset, Refreshing the watchdog, Reading and clearing the SPI status registers. A wake-up event on CAN, LINx, or WKx will generate an interrupt on the INT pin, but will not change the SBC mode.

The configuration options are listed below:

- VCC1 is ON
- VCC2 is fixed as configured in SBC Normal Mode
- VCC3 is fixed as configured in SBC Normal Mode
- CAN mode is fixed as configured in SBC Normal Mode
- LIN mode is fixed as configured in SBC Normal Mode
- WK pins are fixed as configured in SBC Normal Mode
- HS Outputs are fixed as configured in SBC Normal Mode
- Cyclic sense is fixed as configured in SBC Normal Mode
- Cyclic wake is fixed as configured in SBC Normal Mode
- Watchdog is fixed as configured in SBC Normal Mode
- SBC Soft Reset can be triggered
- FOx outputs retain their previous state from SBC Normal Mode

When entering SBC Stop Mode, an interrupt is generated on the INT pin if any wake-source indication flags in **WK_STAT_1** and **WK_STAT_2** are not cleared.

Notes

1. If switches are enabled during SBC Stop Mode (e.g., HSx ON with or without PWM control), the overall SBC current consumption will increase (**Chapter 4.4**).
2. It is not possible to switch directly from SBC Stop Mode to SBC Sleep Mode. Attempting this transition will set the **SPI_FAIL flag** and force the SBC into Restart Mode.
3. When WK1 and WK2 are configured for the alternate measurement function (**WK_MEAS = 1**), these inputs cannot be used as wake-up sources.

5.1.4 SBC Sleep Mode

The SBC Sleep Mode represents the second-level low-power technique, designed to minimize the overall current consumption while still allowing the device to respond to wake-up events or perform autonomous functions (e.g., cyclic sense). In this mode, VCC1 is turned OFF, and therefore the microcontroller is no longer supplied. The VCC2 supply and HSx outputs can be configured to remain enabled if required. All configuration settings must be completed before entering SBC Sleep Mode. A wake-up event on CAN, LINx, or WKx will cause the device to transition via SBC Restart Mode back to SBC Normal Mode, while also indicating the corresponding wake source.

The configuration options are listed below:

- VCC1 is OFF
- VCC2 is fixed as configured in SBC Normal Mode
- VCC3 is fixed or OFF as configured in SBC Normal Mode
- CAN mode changes automatically from ON or Receive Only Mode to wake capable mode or can be selected to be OFF
- CAN must be set to CAN wake capable / CAN off mode before entering SBC Sleep Mode
- LIN mode changes automatically from ON or Receive Only Mode to wake capable mode or can be selected to be OFF
- WK pins are fixed as configured in SBC Normal Mode
- HS Outputs are fixed as configured in SBC Normal Mode
- Cyclic sense is fixed as configured in SBC Normal Mode
- Cyclic wake is not available
- Watchdog is OFF
- FOx outputs are fixed,i.e. the state from SBC Normal Mode is maintained
- As VCC1 is OFF during SBC Sleep Mode, no SPI communication is possible;
- The Sleep Mode entry is signalled in the SPI register **DEV_STAT** with the bit **DEV_STAT**

It is not possible to disable all wake sources while in SBC Sleep Mode. Attempting to do so will set the **SPI_FAIL** flag and force the SBC to enter SBC Restart Mode.

To successfully enter SBC Sleep Mode, all wake-source indication flags in **WK_STAT_1** and **WK_STAT_2** must be cleared beforehand. If these flags are not cleared, the device will immediately wake up, transitioning via SBC Restart Mode to SBC Normal Mode.

All configuration steps must be completed prior to entering Sleep Mode.

Notes

1. If switches (such as HSx outputs) are enabled during SBC Sleep Mode —with or without PWM control— the overall SBC current consumption will increase (see **Chapter 4.4**).
2. The Cyclic Sense function may not operate correctly in cases of over-current, over-temperature, under-voltage, or over-voltage events (if enabled), because the corresponding HS switch will be disabled.
3. When WK1 and WK2 are configured for the alternate measurement function (**WK_MEAS** = 1), they cannot be used as wake-up input sources

5.1.5 SBC Restart Mode

The SBC Restart Mode can be entered for several reasons. Its primary purpose is to reset the microcontroller under specific conditions, including:

- Undervoltage on VCC1 during SBC Normal Mode or SBC Stop Mode.
- Overvoltage on VCC1, if the bit **VCC1_OV_RST** is set and **CFGP** = '1'.
- First incorrect watchdog trigger, applicable only when Config 1, Config 3, or Config 4 is selected (otherwise, the device immediately enters SBC Fail-Safe Mode).
- Wake-up events from SBC Sleep Mode or SBC Fail-Safe Mode, or the release of over-temperature shutdown (TSD2) from SBC Fail-Safe Mode — in these cases, the transition through Restart Mode ensures a defined ramp-up sequence of VCC1 after wake-up.

Upon entering SBC Restart Mode, the device will automatically transition to SBC Normal Mode without any microcontroller intervention. The SBC **MODE** bits are cleared during this process. As illustrated in **Figure 52**, the Reset Output (RO) is pulled low when entering Restart Mode and is released upon transition to Normal Mode after the reset delay time (t_{RD1}). The watchdog timer starts with an extended open window from the rising edge of RO, and the watchdog period setting in the register **WD_CTRL** is reset to its default value '100'.

Exiting SBC Restart Mode does not alter or deactivate the Fail Outputs (FOx).

During SBC Restart Mode, the internal blocks behave as follows:

FOx outputs are activated in the event of a first watchdog-trigger failure (if Config 1 or Config 2 is selected) or upon VCC1 overvoltage detection (if **VCC1_OV_RST** is set).

- VCC1 is ON or ramping up.
- VCC2 is disabled if it was previously enabled.
- VCC3 remains fixed or ramps according to its configuration in SBC Normal Mode.
- CAN is "woken" due to a wake event or remains OFF, depending on the previous SBC and transceiver mode (see **Chapter10**). It is wake-capable if it was in CAN Normal, Receive Only, or Wake-Capable Mode before Restart Mode.
- LIN is "woken" or OFF depending on the previous SBC and transceiver mode (see **Chapter 11**). It is wake-capable if it was in LIN Normal, Receive Only, or Wake-Capable Mode before Restart Mode.
- HS outputs are disabled if they were previously active.
- RO is pulled low throughout SBC Restart Mode.
- SPI communication is ignored by the SBC (i.e., commands are not interpreted).
- Entry into Restart Mode is indicated in the SPI register **DEV_STAT** by the corresponding **DEV_STAT** bits.

Table 7 Reasons for Restart - State of SPI Status Bits after Return to Normal Mode

Prev. SBC Mode	Event	DEV_STAT	WD_FAIL	VCC1_UV	VCC1_OV	VCC1_SC
Normal	1xWatchdog Failure	01	01	x	x	x
Normal	2xWatchdog Failure	01	10	x	x	x
Normal	VCC1 undervoltage reset	01	xx	1	x	x
Normal	VCC1 overvoltage reset	01	xx	x	1	x
Stop	1xWatchdog Failure	01	01	x	x	x
Stop	2xWatchdog Failure	01	10	x	x	x
Stop	VCC1 undervoltage reset	01	xx	1	x	x
Stop	VCC1 overvoltage reset	01	xx	x	1	x
Sleep	Wake-up event	10	xx	x	x	x

Fail-Safe	Wake-up event	01	see “Reasons for Fail Safe, **Table 8**”

Notes

1. An overvoltage event on VCC1 will only lead to SBC Restart Mode if the bit VCC1_OV_RSTis set and if **CFGP** = ‘1’ (Config 1/3).
2. The content of the WD_FAIL bits will depend on the device configuration, e.g. 1 or 2 watchdog failures.

5.1.6 SBC Fail-Safe Mode

The SBC Fail-Safe Mode is designed to bring the system into a safe state under failure conditions by turning off the VCC1 supply and powering down the microcontroller. After a valid wake-up event, the system is able to restart automatically.

The SBC automatically enters Fail-Safe Mode under any of the following conditions:

- After an SBC thermal shutdown (TSD2) (see **Chapter 15.9.3**).
- In case of VCC1 overvoltage, if the bit **VCC1_OV_RST** is set and **CFGP** = ‘0’.
- After the first incorrect watchdog trigger in Config 2 (**CFG** = 1), or after the second incorrect watchdog trigger in Config 4 (**CFG** = 0) (see **Chapter 5.1.1**).
- If VCC1 is shorted to GND (see **Chapter 15.7**).
- After 4 consecutive VCC1 undervoltage events (only if VS > VS,UV, see **Chapter 15.6**).

In this mode, the default wake sources — CAN, LINx, and WK1…WK3 (refer to registers **WK_CTRL_2**, **BUS_CTRL_1,** and **BUS_CTRL_2**) — are activated. At the same time, all wake event flags in WK_STAT_1 are cleared, and every output driver as well as all voltage regulators are switched off. If WK1 and WK2 are configured for the alternate measurement function (WK_MEAS = 1), they remain in measurement configuration when the SBC enters Fail-Safe Mode, meaning they are not enabled as wake sources.

The SBC remains in Fail-Safe Mode until a wake event occurs on one of the default wake sources. To prevent rapid toggling, a typical filter time of 100 ms ($t_{FS,min}$) is applied. Any wake events detected during this period are stored and will automatically trigger entry into SBC Restart Mode after the filter time has elapsed. In the case of a VCC1 over-temperature shutdown (TSD2), the SBC will automatically transition to Restart Mode after a typical delay of 1 s (t_{TSD2}), without requiring a wake event. Exiting Fail-Safe Mode does not deactivate the Fail Output pins.
Functional Behavior in Fail-Safe Mode

During SBC Fail-Safe Mode, the following conditions apply:

- All FOx outputs are activated (see **Chapter 14**).
- VCC1, VCC2, and VCC3 are OFF.
- CAN is wake-capable.
- LINx is wake-capable.
- HS outputs are OFF.
- WK pins are wake-capable via static sense (default 16 µs filter time).
- Cyclic Sense and Cyclic Wake functions are disabled.
- SPI communication is disabled, as VCC1 is OFF.
- Activation of Fail-Safe Mode is indicated in the SPI register **DEV_STAT** by the bits **FAILURE** and DEV_STAT.

Table 8 Reasons for Fail-Safe - State of SPI Status Bits after Return to Normal Mode

Prev. SBC Mode	Failure Event	DEV_ STAT	TSD2	WD_ FAIL	VCC1_ UV	VCC1_ UV_FS	VCC1_ OV	VCC1_ SC
Normal	1 x Watchdog Failure	01	x	01	x	x	x	x
Normal	2 x Watchdog Failure	01	x	10	x	x	x	x
Normal	TSD2	01	1	xx	x	x	x	x
Normal	VCC1 short to GND	01	x	xx	1	x	x	1

Normal	4xVCC1 UV	01	x	xx	1	1	x	x
Normal	VCC1 overvoltage	01	x	xx	x	x	1	x
Stop	1 x Watchdog Failure	01	x	01	x	x	x	x
Stop	2 x Watchdog Failure	01	x	10	x	x	x	x
Stop	TSD2	01	1	xx	x	x	x	x
Stop	VCC1 short to GND	01	x	xx	1	x	x	1
Stop	4xVCC1 UV	01	x	xx	1	1	x	x
Stop	VCC1 overvoltage	01	x	xx	x	x	1	x

Notes
1. An overvoltage event on VCC1 will only lead to SBC Fail-Safe Mode if the bit VCC1_OV_RST is set and if **CFGP** = '0' (Config 2/4).
2. The content of the WD_FAIL bits will depend on the device configuration, e.g. 1 or 2 watchdog failures.
3. See **Chapter 15.6.1** for detailed description of the 4x VCC1 undervoltage behavior.

5.1.7 SBC Development Mode

The SBC Development Mode is intended for use during the module development phase and is particularly beneficial for software development activities.

Compared to the standard SBC User Mode, this mode represents an extended version of the state machine. The device still starts in SBC Init Mode, and all SBC modes and functions remain accessible, with the following distinctions:
- The watchdog timer is disabled and does not require servicing; therefore, no reset will occur due to watchdog timeout.
- SBC Fail-Safe Mode and SBC Restart Mode are not entered as a result of watchdog failure; however, other conditions that trigger these modes remain valid.
- In SBC Init Mode, as well as when transitioning from SBC Init Mode to SBC Normal Mode, the default states of LINx, CAN, and VCC2 are ON instead of OFF.

The SBC automatically enters Development Mode when the FO3/TEST pin is held LOW during SBC Init Mode. Voltage monitoring begins once VS > $V_{POR,f}$. The Development Mode is configured and maintained if any SPI command is transmitted while FO3/TEST remains LOW during SBC Init Mode. If the FO3/TEST pin is held HIGH for a duration longer than t_{TEST} during this monitoring period, the device will not enter Development Mode.

Once activated, the SBC remains in Development Mode under all operating conditions and can only exit this mode by powering down the device (VS < $\mathbf{V_{POR,f}}$).

Note: The absolute maximum ratings of the FO3/TEST pin must be observed. To enhance pin robustness during debugging or programming, it is recommended to insert a series resistor between the FO3/TEST pin and the external connector (see **Figure 66**).

5.2 Wake Features

Following wake sources are implemented in the device:
- Static Sense: WK inputs are permanently active (see **Chapter 12**)
- Cyclic Sense: WK inputs only active during on-time of cyclic sense period (see below)
- Cyclic Wake: internal wake source controlled via internal timer (see below)
- CAN wake: Wake-up via CAN message (see **Chapter 10**)
- LIN wake: Wake-up via LIN message (see **Chapter 11**)

5.2.1 Cyclic Sense

The cyclic sense function is designed to minimize the quiescent current consumption of both the device and the overall application. In this configuration, one or more high-side drivers are periodically activated under the

control of **TIMER1_CTRL** and **TIMER2_CTRL**. These high-side drivers provide power to external circuits such as switches or resistor networks, which are connected to one or more wake inputs (see **Figure 5**). During the active phase of each cyclic sense period, any signal transition detected on a WKx input triggers a wake event. Depending on the current SBC operating mode, this event either pulls the INT pin low (in Normal Mode or Stop Mode) or wakes the SBC by enabling VCC1 (after Sleep Mode or Fail-Safe Mode).

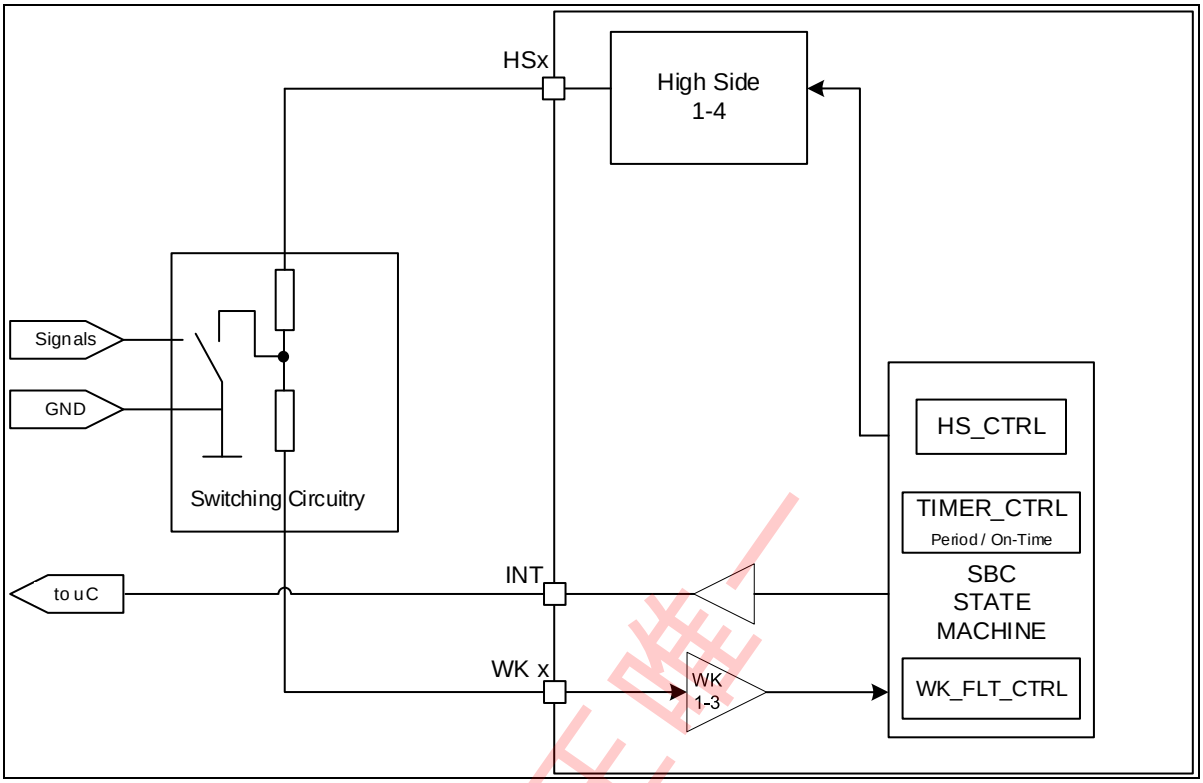


Figure 5 Cyclic Sense Working Principle

5.2.1.1 Configuration and Operation of Cyclic Sense

The configuration sequence for the cyclic sense function is illustrated in Figure 6. All configuration steps must be completed before setting the on-time parameter in the TIMERx_CTRL registers. The options “OFF/LOW” and “OFF/HIGH” define the default voltage level of the corresponding high-side (HS) driver prior to activating the cyclic sense function. This setting helps to prevent unintended wake events that could occur due to voltage transitions when cyclic sensing begins.The cyclic sense operation (TimerX) starts automatically once the on-time value is configured, regardless of the specific high-side or filter assignments. Therefore, the selection of the appropriate timer (refer to Configuration C/D in **Chapter 12.2.1**) must be completed before enabling the timer.

The recommended configuration sequence is as follows:

- Set the initial output level.
- Assign a timer to the corresponding HSx output(s).
- Configure the filter timing and WK input pins.
- Define the timer period and on-time parameters.

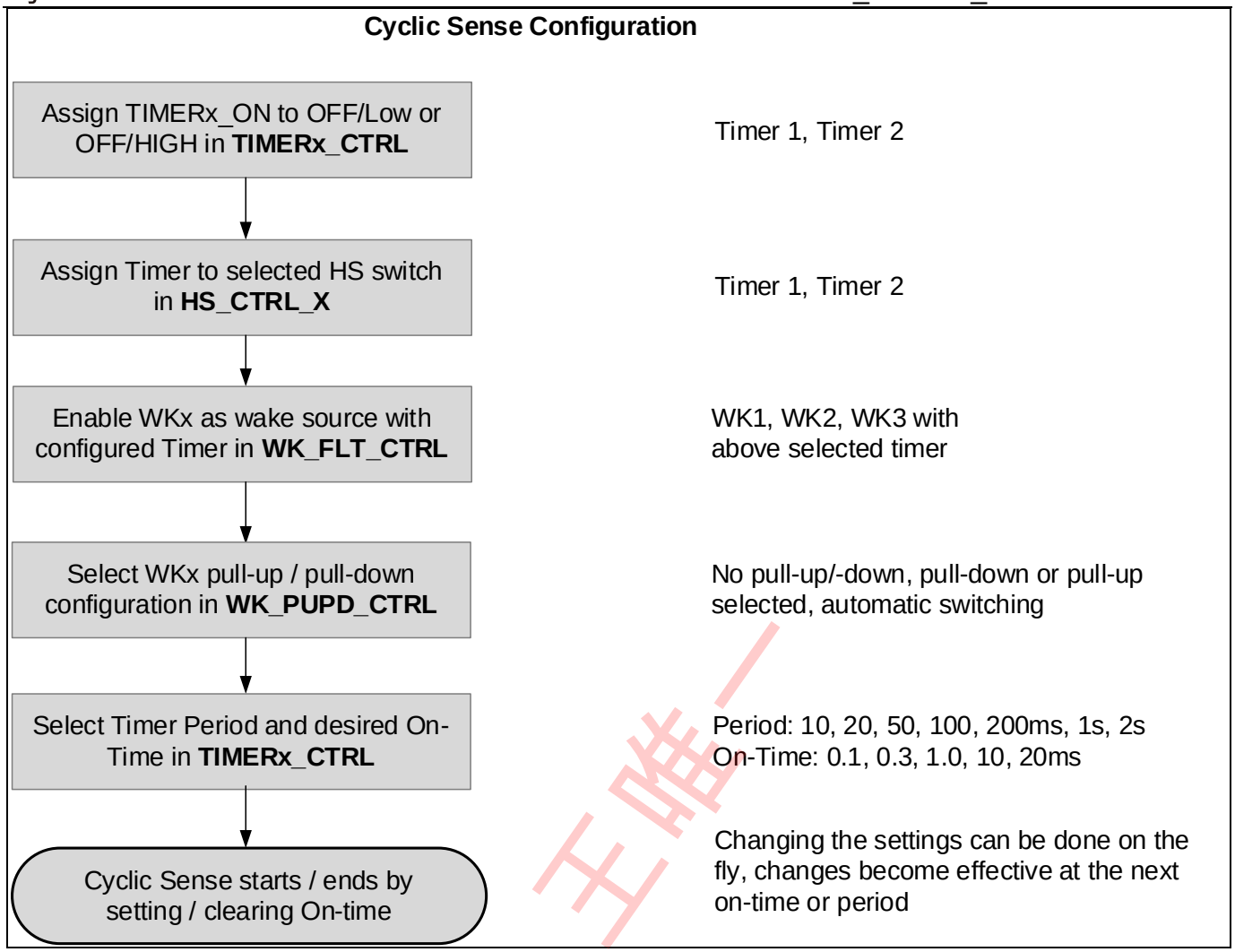


Figure 6 Cyclic Sense: Configuration and Sequence

Note: All configurations of period and on-time can be selected. However, recommended on-times for cyclic sense are 0.1ms, 0.3ms and 1ms. The SPI_FAIL will be set if the on-time is longer than the period.

During cyclic sense operation, the initial sample of the WK input level (either HIGH or LOW) is stored as a reference for the subsequent cycle. If a change in the WK input level is detected between the first and second cycles—specifically during the on-time of the second cycle—a wake event will be generated. This event results in either a wake-up from SBC Sleep Mode or an interrupt in SBC Normal Mode or SBC Stop Mode.

To prevent unintended wake-ups caused by transient signals or electromagnetic interference (EMC) disturbances, a filter time of 16 µs is implemented. The filter period (tFWK1) starts immediately after the selected on-time ends, and a wake signal is validated only if:

- The input voltage does not cross the typical switching threshold level of 3 V during the filter period (i.e., the signal remains stable at either HIGH or LOW)
- A change in the input level has occurred compared to the previous cycle.

When a cyclic sense wake event is detected, the corresponding flag (WK1_WU, WK2_WU, or WK3_WU) is set. During cyclic sense operation, the **WK_LVL_STAT** register is updated only with the sampled voltage levels of the WKx pins in SBC Normal Mode or SBC Stop Mode.

The sampling process and its various operational scenarios are illustrated in **Figure 7** to **Figure 9**. The functional behavior in SBC Stop Mode and SBC Sleep Mode is identical, except that in Stop Mode, an INT signal is triggered to indicate a change in WK input levels, whereas in Sleep Mode, the VCC1 supply is enabled instead.

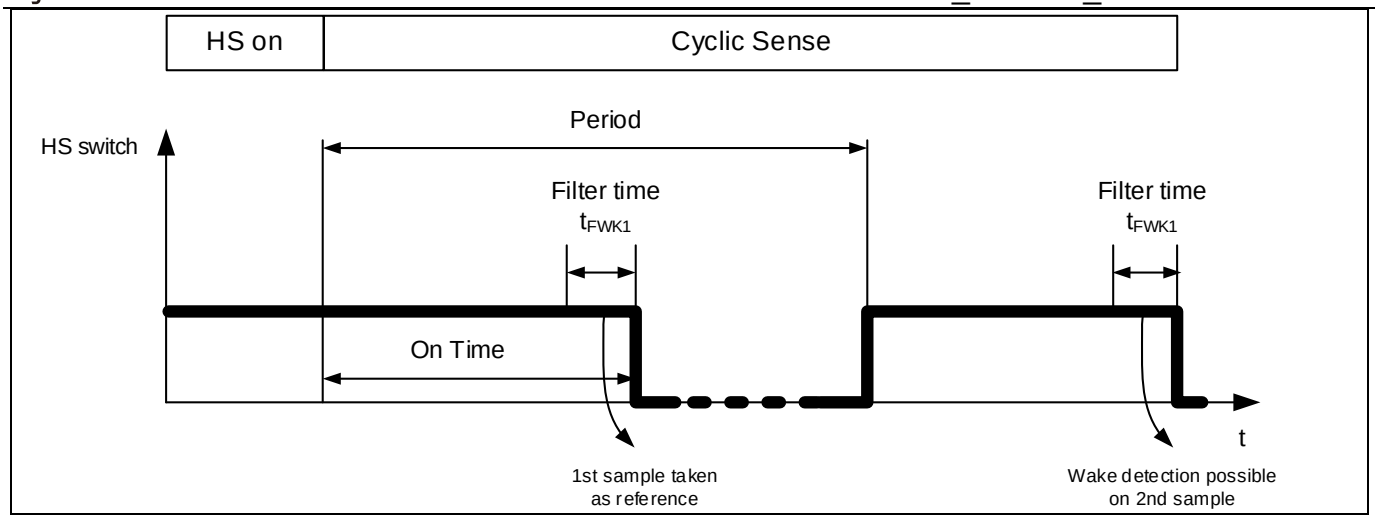


Figure 7 Wake Input Timing

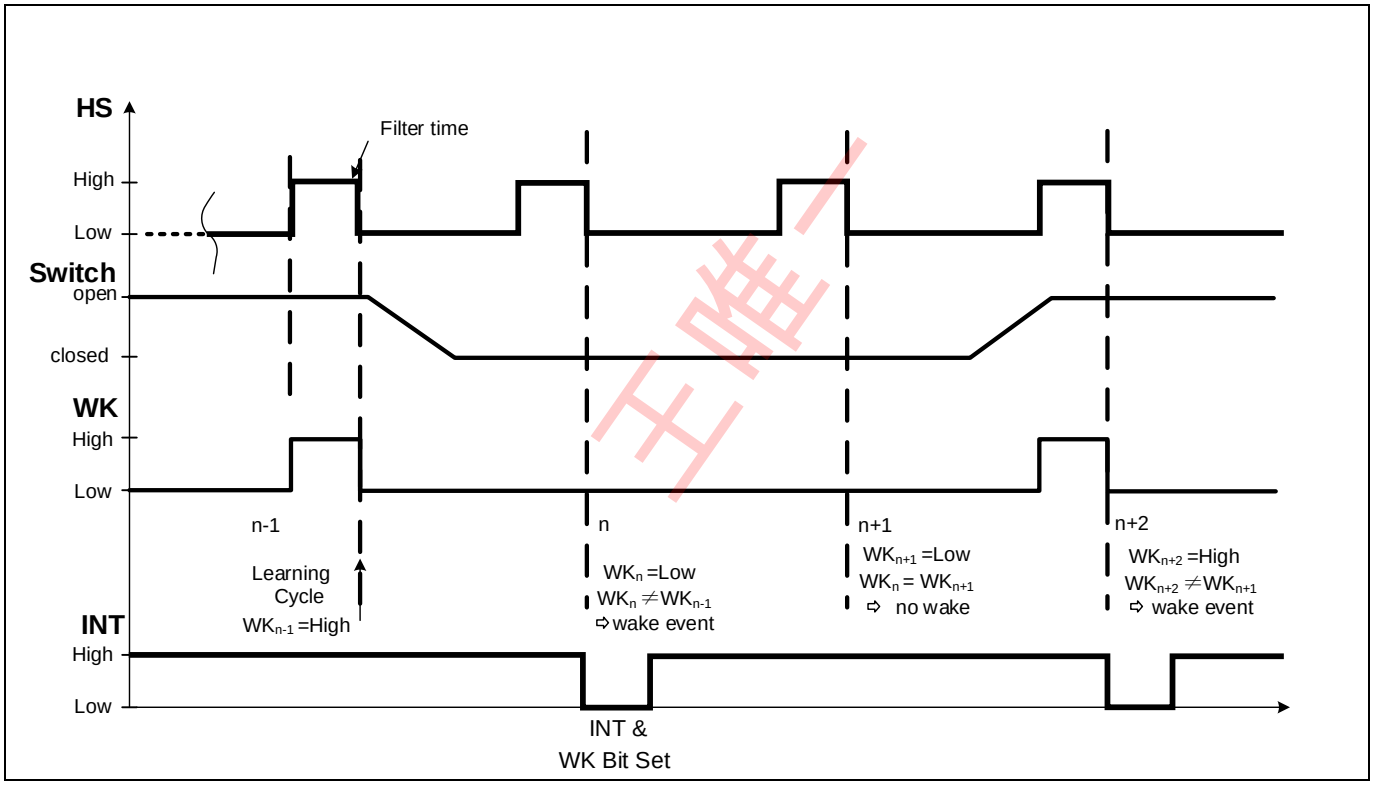


Figure 8 Cyclic Sense Example in SBC Stop Mode, HSx starts “OFF”/LOW, GND based WKx input

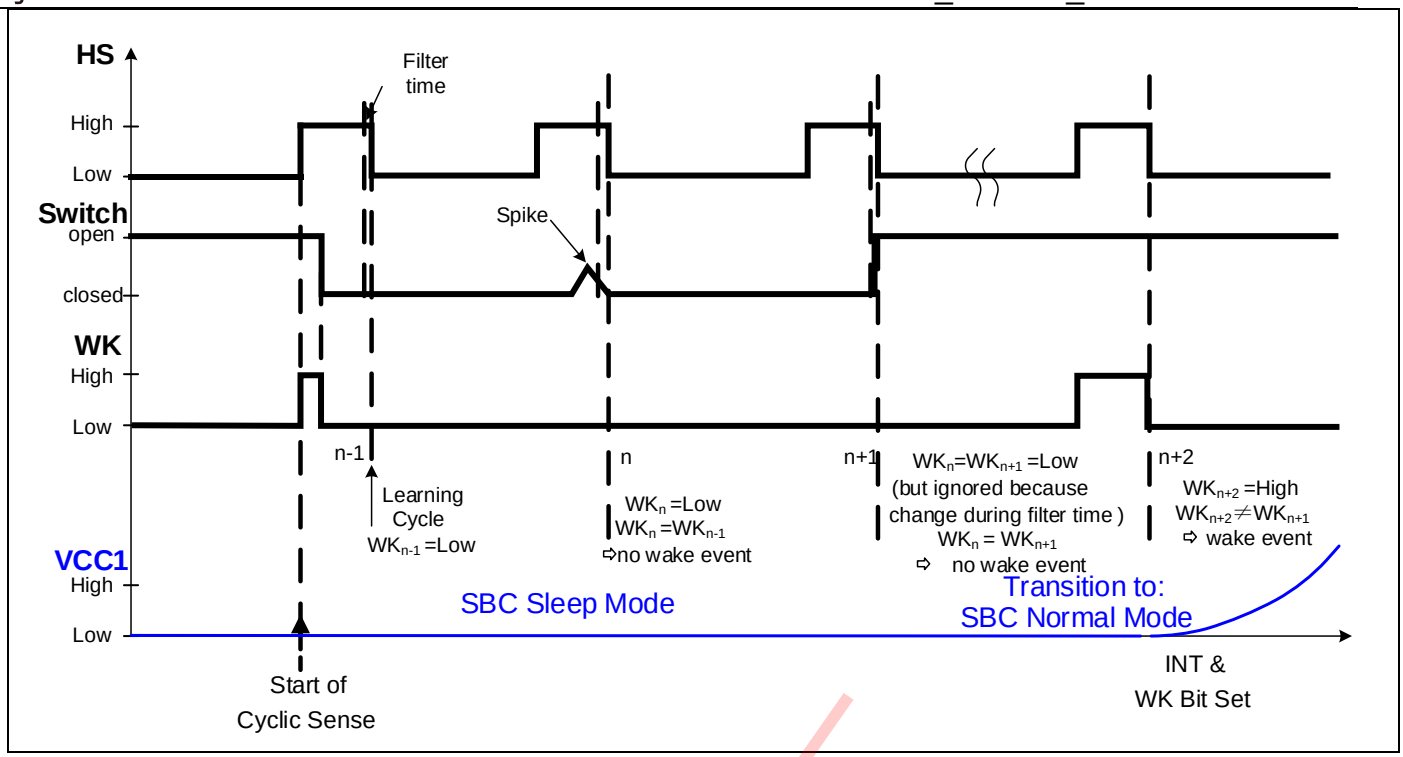


Figure 9 Cyclic Sense Example in SBC Sleep Mode, GND based WKx input

The cyclic sense function will not work properly anymore in case of following conditions:

- in case SBC Fail-Safe Mode is entered: The respective HS Switch will be disabled and the respective wake pin will be changed to static sensing
- In SBC Normal, Stop, or Sleep Mode in case of an overcurrent, overtemperature, under- or overvoltage (in case function is selected) event: the respective HS switch will be disabled

Note: The internal timers for cyclic sense are not disabled automatically in case the HS switch is turned off due to above mentioned failures.This must be considered to avoid loss of wake events.

5.2.1.2 Cyclic Sense in Low Power Mode

When cyclic sense is intended for operation in SBC Stop Mode or SBC Sleep Mode, it must first be enabled while the device is in SBC Normal Mode before transitioning to the respective low-power mode. A wake event triggered by cyclic sense will set the corresponding status bit (WK1_WU, WK2_WU, or WK3_WU). In Stop Mode, such a wake event will generate an interrupt signal, whereas in Sleep Mode, the event will cause the device to transition via Restart Mode back to Normal Mode. Prior to re-entering SBC Sleep Mode, the wake status registers (**WK_STAT_1** and **WK_STAT_2**) must be cleared. If the system attempts to enter Sleep Mode while any wake flag (e.g., WKx_WU) remains uncleared, the SBC will immediately wake up from Sleep Mode, passing through Restart Mode and returning to Normal Mode, with a reset being issued. The corresponding WKx_WU bit is recognized as the wake source. This mechanism ensures that no wake event is lost during mode transitions.

5.2.2 Cyclic Wake

The Cyclic Wake feature is designed to minimize the overall quiescent current of both the device and the application system. In this mode, one or both internal timers can be configured as internal wake-up sources, periodically generating interrupts while the device operates in SBC Normal Mode or SBC Stop Mode.

The correct configuration procedure for the cyclic wake function is illustrated in **Figure 10** and must be performed in the following sequence:

- Disable all timers to prevent unintended interrupts during the configuration process.

- Enable Timer1 and/or Timer2 as wake-up sources by setting the corresponding bits in the **WK_CTRL_1** register.
- Configure the timer period for Timer1 and/or Timer2. An on-time value must also be defined to initiate cyclic wake operation, even though this value is not functionally used during the process

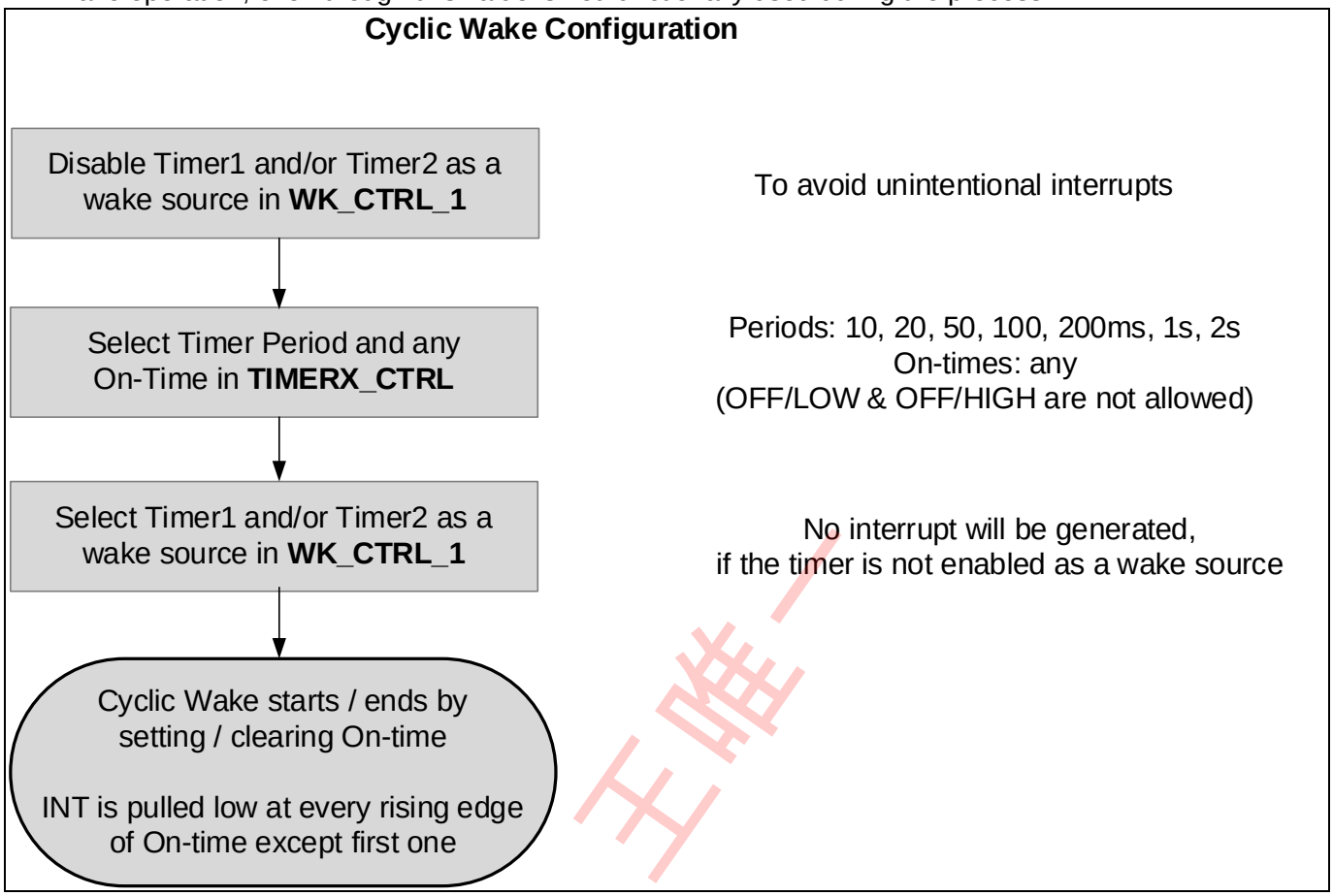


Figure 10 Cyclic Wake: Configuration and Sequence

As in cyclic sense, the cyclic wake function will start as soon as the on-time is configured. An interrupt is generated for every start of the on time except for the very first time when the timer is started

5.2.3 Internal Timer

The integrated Timer1 and Timer2 are typically used to wake up the microcontroller periodically (cyclic wake) or to perform cyclic sense on the wake inputs. Therefore, the timers can be mapped to the dedicated HS switches by SPI (via **HS_CTRL1**...2).

Following periods and on-times can be selected via the register **TIMER1_CTRL** and **TIMER2_CTRL** respectively:

- Period: 10ms / 20ms / 50ms / 100ms / 200ms / 1s / 2s
- On time: 0.1ms / 0.3ms / 1.0ms / 10ms / 20ms / OFF at HIGH or LOW

5.3 Supervision Features

The device offers various supervision features to support functional safety requirements. Please see **Chapter 15** for more information.

5.4 Partial Networking on CAN

5.4.1 CAN Partial Networking - Selective Wake Feature

The CAN Partial Networking feature allows selective wake-up of the system via the CAN interface, thereby reducing overall power consumption while maintaining bus communication awareness. This feature can be activated during SBC Normal Mode, SBC Sleep Mode, and SBC Stop Mode. For SBC Sleep Mode, the

Partial Networking function must be enabled before the device transitions into Sleep Mode. Similarly, for SBC Stop Mode, the feature must be activated prior to entering the Stop Mode.

Two distinct detection mechanisms are available for CAN-based wake-up:

- WUP (Wake-Up Pattern) – A basic CAN wake-up mechanism that detects the presence of two consecutive dominant pulses on the CAN bus, as defined in ISO 11898‑2:2016.
- WUF (Wake-Up Frame) – An enhanced wake-up mechanism that triggers when a received CAN frame matches a user-defined message filter configured in the SBC via the SPI interface.

The default CAN baud rate is set to 500 kBaud. In addition to commonly used baud rates such as 125 kBaud and 250 kBaud, other baud rates up to 1 MBaud are also supported. For detailed configuration procedures and register-level settings, refer to **Chapter 16.5.2** and **Chapter 16.5.3.**

5.4.2 SBC Partial Networking Function

The CAN Partial Networking Modes are shown in this figure.

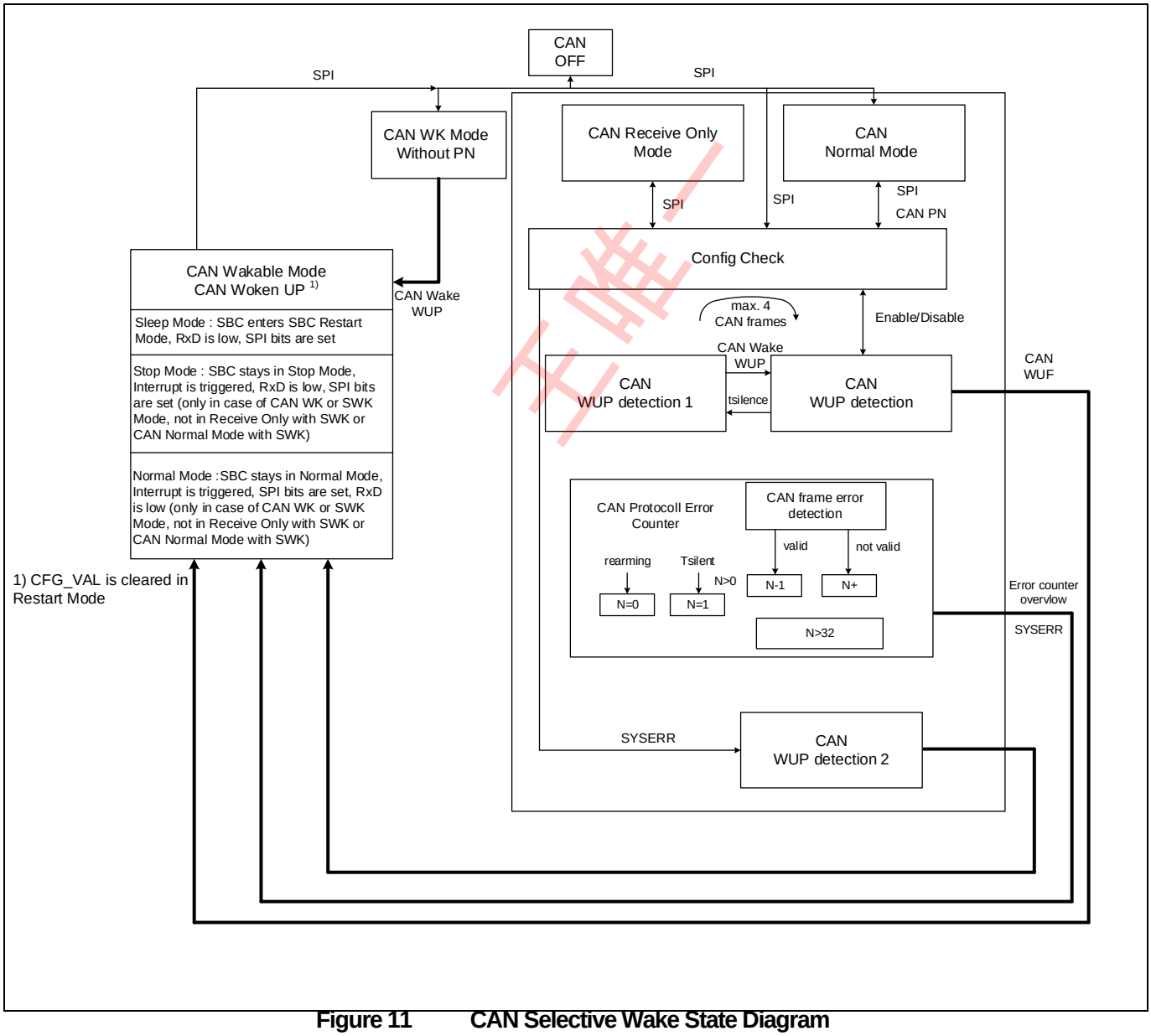


Figure 11 CAN Selective Wake State Diagram

5.4.2.1 Activation of SWK

Below figure shows the principal of the SWK activation.

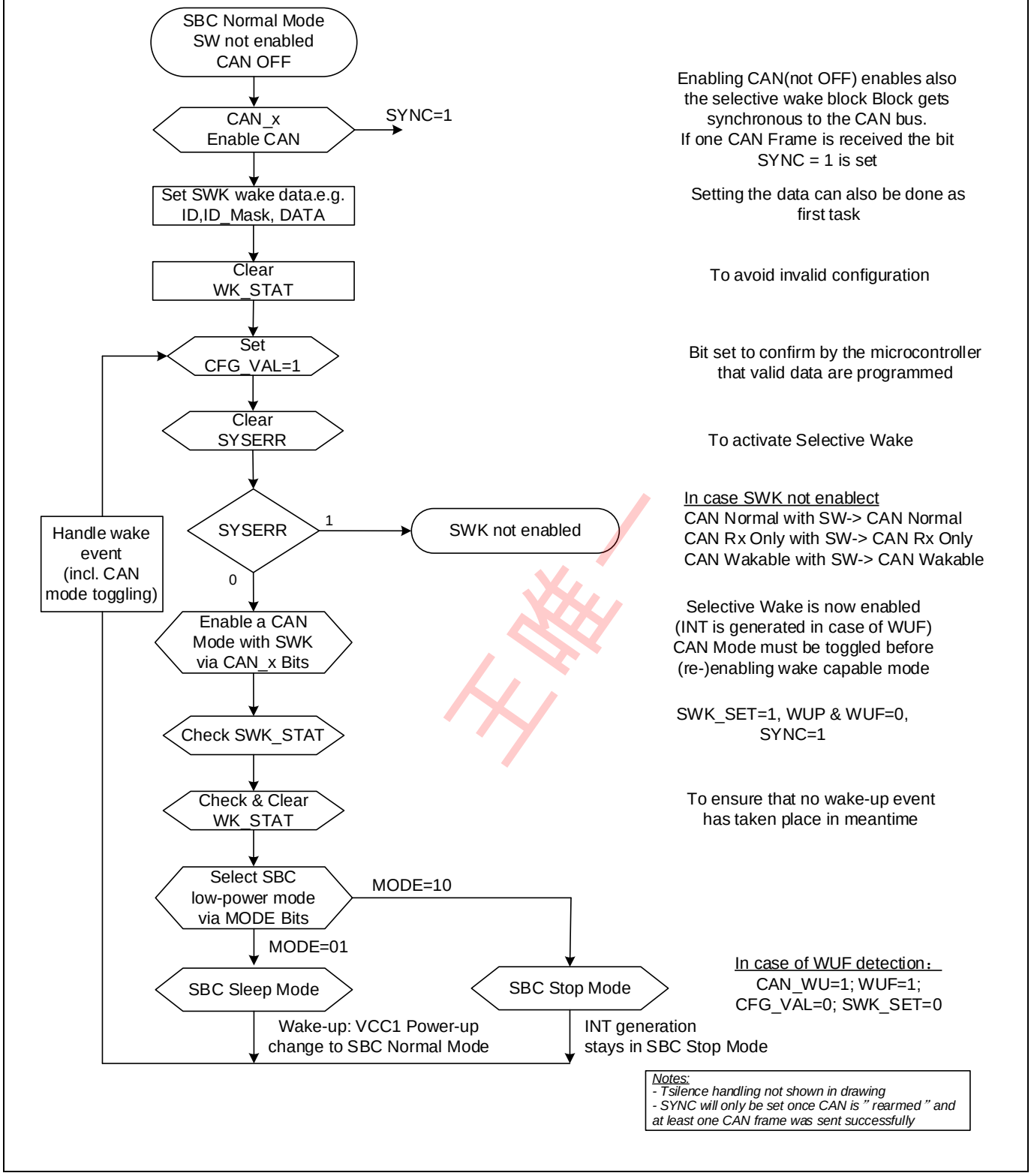


Figure 12 Flow for activation of SWK

Note: The CAN SWK feature is only available for GD33AP236x-3 variants.

5.4.2.2 Wake-up Pattern (WUP)

A WUP is signaled on the bus by two consecutive dominant bus levels for at least t_{WAKE1}, each separated by a recessive bus level.

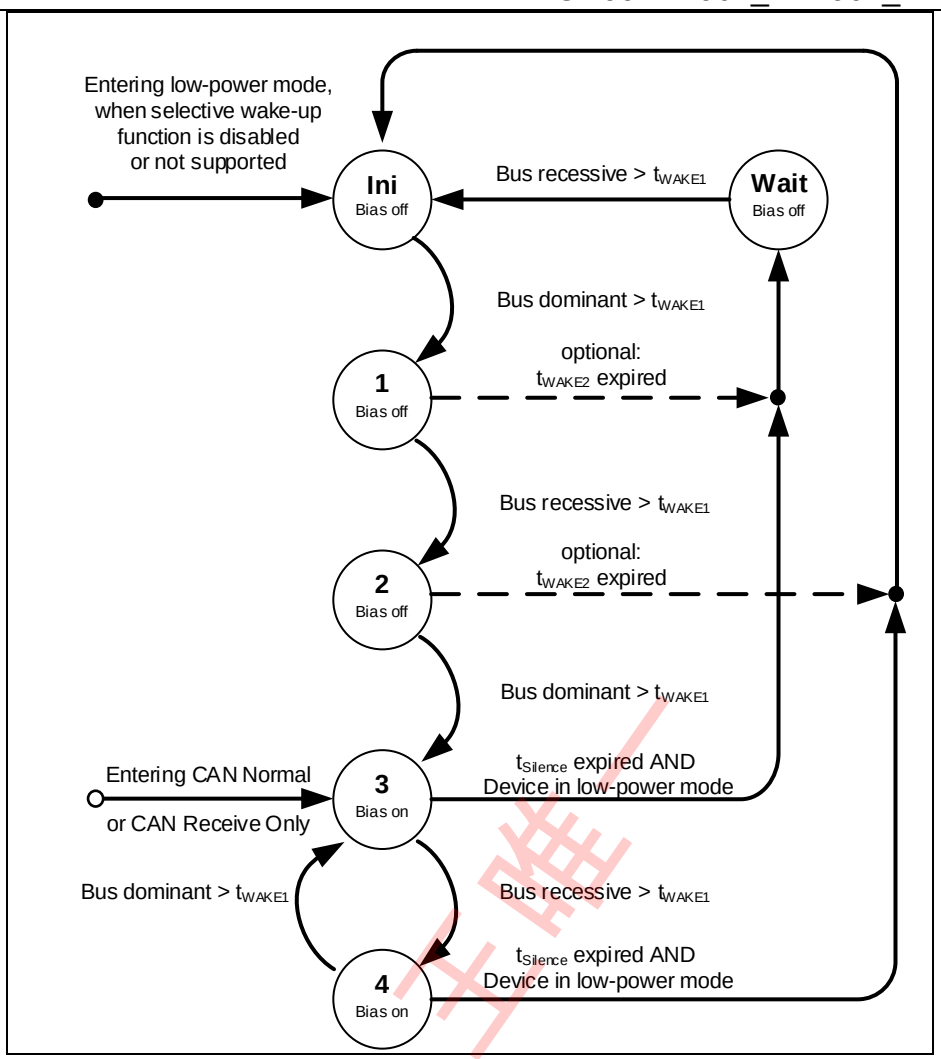


Figure 13 WUP detection following the definition in ISO 11898-2:2016

5.4.2.3 Wake-up Frame (WUF)

The Wake-up Frame (WUF) detection is implemented in accordance with ISO 11898-2:2016. Only CAN frames compliant with ISO 11898-1 are considered as potential wake-up frames.

A bus wake-up shall be performed if the Selective Wake-up function is enabled and a valid WUF has been received. The transceiver may ignore up to four consecutive CAN data frames that start after switching on the bias.

A received frame is a “valid WUF” in case all of the following conditions are met:

- The ID of the received frame exactly matches the configured ID in the relevant bit positions defined by the ID Mask. The ID and the ID Mask might have either 11 bits or 29 bits.
- The DLC of the received frame is exactly matching the configured DLC.
- In case DLC is greater than 0, the data field of the received frame has at least one bit set in a bit position where also in the configured Data Mask the corresponding bit position is set.
- No error exists according to ISO 11898-1, excepting errors which are signalled in the ACK field and EOF field.

5.4.2.4 CAN Protocol Error Counter

The CAN Protocol Error Counter monitors the integrity of received CAN frames during operation. The counter is incremented whenever a bit stuffing, CRC, or form error is detected according to ISO 11898-1. If a frame has been received and is valid up to the end of the CRC field while the counter value is not zero, the counter is decremented by one.

If the counter reaches a value of 31, the following actions are performed upon the next increment:

- The Selective Wake function is disabled.
- The CAN transceiver is woken.
- The SYSERR flag is set, and the error counter value of 32 can be read.

On each increment or decrement of the counter, the decoder unit waits for at least 6 and at most 10 recessive bits before considering a dominant bit as a new start-of-frame.

The error counter is enabled under the following conditions:

- Whenever the CAN is in Normal Mode, Receive-Only Mode, or in WUF detection state.
- At the transition from WUF detection to WUP detection 1 (after $t_{SILENCE}$ expiration, while SWK is correctly enabled).
- When WUF detection state is entered (the counter starts from 0 when SWK is enabled).
- At SBC or CAN rearming (when exiting the woken state).
- When the CAN Mode bits are selected '000', '100' (CAN OFF) or '001' (Wake capable without SWK function enabled).
- While CAN_FD_EN = '1' and DIS_ERR_CNT = '1' (the counter is cleared and remains cleared when these two bits are set in the SPI registers).

The error counter is frozen after a wake-up while being in the woken state.

The current counter value can be read from the **ECNT** bits.

5.4.3 Diagnoses Flags

5.4.3.1 PWRON/RESET-FLAG

The power-on reset can be detected and read by the **POR** bit in the SBC Status register.

The VS power on resets all register in the SBC to reset value. SWK is not configured.

5.4.3.2 BUSERR-Flag

Bus Dominant Time-out detection is implemented and signaled by CAN_Fail_x in register **BUS_STAT_1**.

5.4.3.3 TXD Dominant Time-out flag

TXD Dominant timeout is shown in the SPI bit CAN_FAIL_x in register **BUS_STAT_1**.

5.4.3.4 WUP Flag

The WUP bit in the **SWK_STAT** register shows that a Wake-Up Pattern (WUP) has caused a wake of the CAN transceiver. It can also indicate an internal mode change from WUP detection 1 state to WUF detection after a valid WUP.

In the following case the bit is set:

- SWK is activated: due to $t_{SILENCE}$,the CAN changes into the state WUP detection 1. If a WUP is detected in this state, then the **WUP** bit is set.
- SWK is deactivated: the **WUP** bit is set if a WUP wakes up the CAN. In addition, the **CAN_WU** bit is set.
- in case WUP is detected during WUP detection 2 state (after a SYSERR) the bits **WUP** and **CAN_WU** are set.

The **WUP** bit is cleared automatically by the SBC at the next rearming of the CAN transceiver.

Note: It is possible that WUF and WUP bit are set at the same time if a WUF causes a wake out of SWK, by setting the interrupt or by restart out of SBC Sleep Mode. The reason is because the CAN has been in WUP detection 1 state during the time of SWK mode (because of $t_{SILENCE}$). See also **Figure 11**.

5.4.3.5 WUF Flag (WUF)

The WUF bit in the **SWK_STAT** register shows that a Wake-Up frame (WUF) has caused awake of the CAN block. In SBC Sleep Mode this wake causes a transition to SBC Restart Mode, in SBC Normal Mode and in SBC Stop Mode it causes an interrupt. Also in case of this wake the bit **CAN_WU** in the register **WK_STAT_1** is set.

The **WUF** bit is cleared automatically by the SBC at the next rearming of the CAN SWK function.

5.4.3.6 SYSERR Flag (SYSERR)

The bit SYSERR is set in case of an configuration error and in case of an error counter overflow. The bit is only updated (set to '1') if a CAN mode with SWK is enabled via CAN_x. If **INT_ GLOBAL** is set, then an interrupt is triggered on INTN every time **SYSERR** is set.

When programming selective wake via CAN_x, SYSERR = '0' signals that the SWK function has been enabled. The bit can be cleared via SPI. The bit is '0' after Power on Reset of the SBC.

5.4.3.7 Configuration Error

A configuration error sets the SYSERR bit to '1'. When enabling SWK via the bits CAN_x a config check is done. If the check is successful SWK is enabled, the bit SYSERR is set to '0'. In SBC Normal Mode it is also possible to detect a Configuration Error while SWK is enabled. This will occur if the **CFG_VAL** bit is cleared, e.g. by changing the SWK registers (from address 010 0001 to address 011 0011). In SBC Stop Mode and SBC Sleep Mode this is not possible as the SWK registers can not be changed.

Configuration Check:
in SBC Restart Mode, the **CFG_VAL** bit is cleared by the SBC. If the SBC Restart Mode was not triggered by a WUF wake up from SBC Sleep Mode and the CAN was with SWK enabled, than the **SYSERR** bit will be set. The SYSERR bit has to be cleared by the microcontroller.

The SYSERR bit cannot be cleared when CAN_2 is '1' and below conditions occur:

- Data valid bit not set by microcontroller,i.e. **CFG_VAL** is not set to '1'. The **CFG_VAL** bit is reset after SWK wake and needs to be set by the microcontroller before activation SWK again.
- **CFG_VAL** bit reset by the SBC when data are changed via SPI programming. (Only possible in SBC Normal Mode)

Note: The SWK configuration is still valid if only the **SWK_CTRL** register is modified.

5.4.3.8 CAN Bus Timeout-Flag (CANTO)

In CAN WUF detection and CAN WUP detection 2 state the bit CANTO is set to '1' if the time $t_{SILENCE}$ expires. The bit can be cleared by the microcontroller. If the interrupt function for CANTO is enabled then an interrupt is generated in SBC Stop or SBC Normal Mode when the CANTO set to '1'. The interrupt is enabled by setting the bit **CANTO_ MASK** to '1'. Each CANTO event will trigger a interrupt even if the CANTO bit is not cleared. There is no wake out of SBC Sleep Mode because of CAN time-out.

5.4.3.9 CAN Bus Silence-Flag (CANSIL)

In CAN WUF detection and CAN WUP detection 2 state the bit CANSIL is set to '1' if the time $t_{SILENCE}$ expires. The CANSIL bit is set back to '0' with a WUP. With this bit the microcontroller can monitor if there is activity on the CAN bus while being in SWK Mode. The bit can be read in SBC Stop and SBC Normal Mode.

5.4.3.10 SYNC-FLAG (SYNC)

The bit SYNC shows that SWK is working and synchronous to the CAN bus. To get a SYNC bit set it is required to enable the CAN to CAN Normal or in Receive Only Mode or in WUF detection. It is not required to enable the CAN SWK Mode.

The bit is set to '1' if a valid CAN frame has been received (no CRC error and no stuffing error). It is set back to '0' if a CAN protocol error is detected. When switching into SWK mode the SYNC bit indicates to the microcontroller that the frame detection is running and the next CAN frame can be detected as a WUF, CAN

wake-up can now be handled by the SBC. It is possible to enter a SBC low-power mode with SWK even if the bit is not set to '1', as this is necessary in case of a silent bus.

5.4.3.11 SWK_SET FLAG (SWK_SET)

The SWK_SET bit is set to signalize the following states (see also **Figure 11**):

- when SWK was correctly enabled in WUF Detection state,
- when SWK was correctly enabled when in WUP Detection 1 state,
- after a SYSERR before a wake event in WUP Detection 2 state,

The bit is cleared under following conditions:

- after a wake-up (ECNT overflow,WUP in WUP detection 2, WUF in WUF detection)
- if CAN_2 is cleared

5.4.4 SBC Modes for Selective Wake (SWK)

The SBC mode is selected via the **MODE** bits as described in **Chapter 5.1**.

The mode of the CAN transceiver needs to be selected in SBC Normal Mode. The CAN mode is programmed via the bits CAN_0, CAN_1 and CAN_2. In the low-power modes (SBC Stop, SBC Sleep) the CAN mode can not be changed via SPI.

The detailed SBC state machine diagram including the CAN selective wake feature is shown in **Figure 3**.

The application must now distinguish between the normal CAN operation an the selective wake function:

- WK Mode: This is the normal CAN wake capable mode without the selective wake function
- SWK Mode: This is the CAN wake capable mode with the selective wake function enabled

Figure 14 shows the possible CAN transceiver modes.

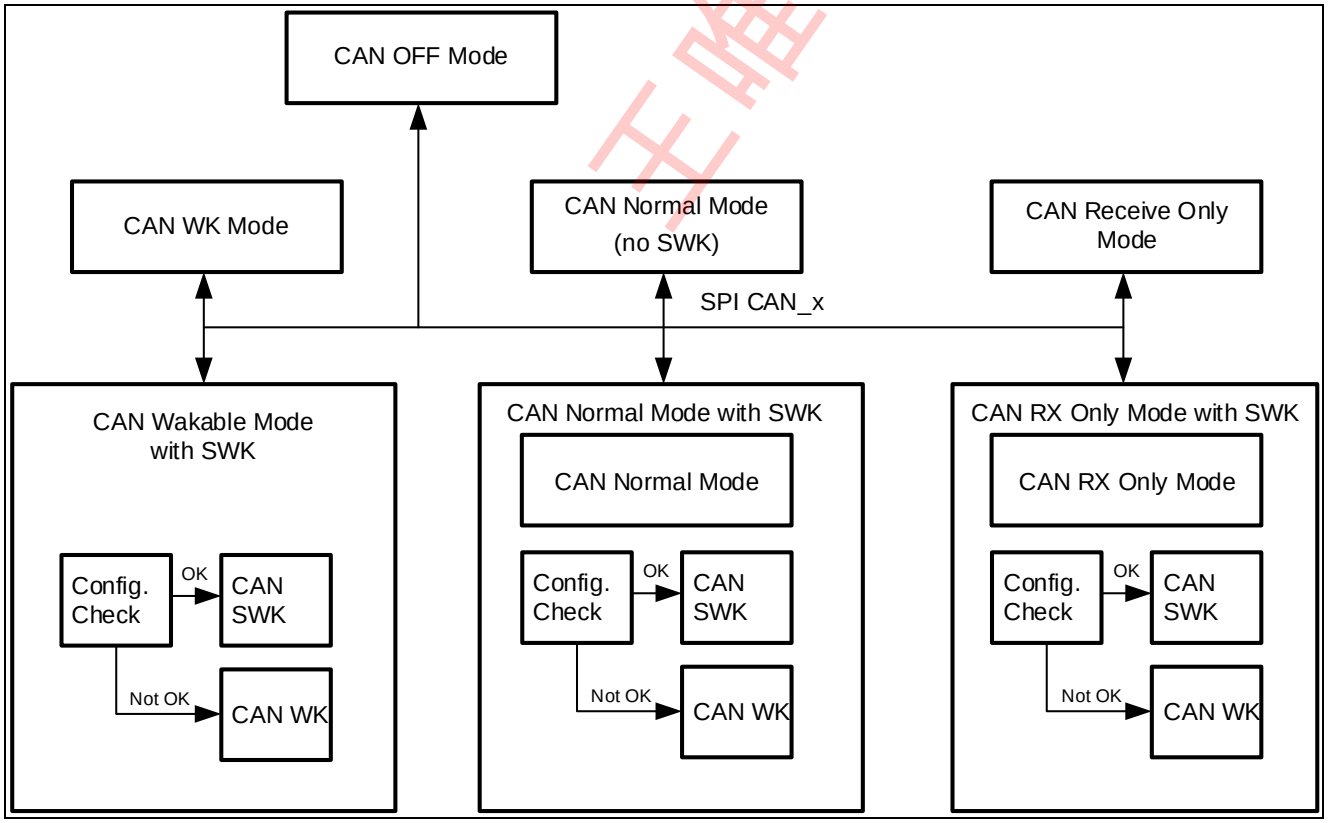


Figure 14 CAN SWK State Diagram

5.4.4.1 SBC Normal Mode with SWK

In SBC Normal Mode the CAN Transceiver can be switched into the following CAN Modes

- CAN OFF
- CAN WK Mode (without SWK)
- CAN SWK Mode
- CAN Receive Only (No SWK activated)
- CAN Receive Only Mode with SWK

- CAN Normal Mode (No SWK activated)
- CAN Normal Mode with SWK

In the CAN Normal Mode with SWK the CAN Transceiver works as in SBC Normal Mode, so bus data is received through RXD, data is transmitted through TXD and sent to the bus. In addition the SWK block is active. It monitors the data on the CAN bus, updates the error counter and sets the **CANSIL** flag if there is no communication on the bus.
It will generate an CAN Wake interrupt in case a WUF is detected (RXD is not pulled to LOW in this configuration).

In CAN Receive Only Mode with SWK, CAN data can be received on RXD and SWK is active, no data can be sent to the bus.

The bit **SYSERR** = '0' indicates that the SWK function is enabled, and no frame error counter overflow is detected.

Table 9 CAN Modes selected via SPI in SBC Normal Mode

CAN Mode	CAN_2	CAN_1	CAN_0
CAN OFF	0	0	0
CAN WK Mode (no SWK)	0	0	1
CAN Receive Only (no SWK)	0	1	0
CAN Normal Mode (no SWK)	0	1	1
CAN OFF	1	0	0
CAN SWK Mode	1	0	1
CAN Receive Only with SWK	1	1	0
CAN Normal Mode with SWK	1	1	1

When reading back CAN_x the programmed mode is shown in SBC Normal Mode. To read the real CAN mode the bits **SYSERR**, **SWK_SET** and **CAN** have to be evaluated. A change out of SBC Normal Mode can change the CAN_0 and CAN_1 bits.

5.4.4.2 SBC Stop Mode with SWK

In SBC Stop Mode the CAN Transceiver can be operated with the following CAN Modes

- CAN OFF
- CAN WK Mode (no SWK)
- CAN SWK Mode
- CAN Receive Only (no SWK)
- CAN Receive Only with SWK
- CAN Normal Mode (no SWK)
- CAN Normal Mode with SWK

To enable CAN SWK Mode the CAN has to be switched to "CAN Normal Mode with SWK", "CAN Receive Only Mode with SWK" or to "CAN SWK Mode" in SBC Normal Mode before sending the SBC to SBC Stop Mode. The bit SYSERR='0' indicates that the SWK function is enabled. The table shows the change of CAN Mode when switching from SBC Normal Mode to SBC Stop Mode.

Note: CAN Receive Only Mode in SBC Stop Mode is implemented to also enable pretended networking (Partial networking done in the microcontroller).

Table 10 CAN Modes change when switching from SBC Normal Mode to SBC Stop Mode

Programmed CAN Mode in SBC Normal Mode	CAN_x bits	SYSERR bit	CAN Mode in SBC Stop Mode	CAN_x bits
CAN OFF	000	0	CAN OFF	000
CAN WK Mode (no SWK)	001	0	CAN WK Mode (no SWK)	001

CAN Receive Only (no SWK)	010	0	CAN Receive Only (no SWK)	010
CAN Normal Mode (no SWK)	011	0	CAN WK Mode (no SWK)	011
CAN OFF	100	0	CAN OFF	100
CAN SWK Mode	101	0	CAN SWK Mode	101
CAN SWK Mode	101	1	CAN WK Mode (no SWK)	101
CAN Receive Only with SWK	110	0	CAN Receive Only with SWK	110
CAN Receive Only with SWK	110	1	CAN Receive Only (no SWK)	110
CAN Normal Mode with SWK	111	0	CAN Normal Mode with SWK	111
CAN Normal Mode with SWK	111	1	CAN Normal Mode (no SWK)	111

Note: When SYSERR is set then WUF frames will not be detected, i.e. the selective wake function is not activated (no SWK), but the MSB of CAN mode is not changed in the register.

5.4.4.3 SBC Sleep Mode with SWK

In SBC Sleep Mode the CAN Transceiver can be switched into the following CAN Modes

- CAN OFF
- CAN WK Mode (without SWK)
- CAN SWK Mode

To enable “CAN SWK Mode” the CAN has to be switched to “CAN Normal Mode with SWK”, “CAN Receive Only Mode with SWK” or to “CAN SWK Mode” in SBC Normal Mode before sending the device to SBC Sleep Mode. The table shows the change of CAN mode when switching from SBC Normal Mode to Sleep Mode.

A wake from Sleep Mode with Selective Wake (Valid WUF) leads to Restart Mode. In Restart Mode the CFG_VAL bit will be cleared by the SBC, the SYSERR bit is not set. In the register CAN_x the programmed CAN SWK Mode (101) can be read.

To enable the CAN SWK Mode again and to enter SBC Sleep Mode the following sequence can be used; Program a CAN Mode different from CAN SWK Mode (101, 110, 111), set the CFG_VAL, CLEAR SYSERR bit, Set CAN_x bits to CAN SWK Mode (101), switch SBC to Sleep Mode.

To enable the CAN WK Mode or CAN SWK Mode again after a wake on CAN a rearming is required for the CAN transceiver to be wake capable again. The rearming is done by programming the CAN into a different mode with the CAN_x bit and back into the CAN WK Mode or CAN SWK Mode. To avoid lock-up when switching the SBC into Sleep Mode with an already woken CAN transceiver, the SBC does an automatic rearming of the CAN transceiver when switching into Sleep Mode. So after switching into Sleep Mode the CAN transceiver is either in CAN SWK Mode or CAN WK Mode depending on CAN_x setting and SYSERR bit (If CAN is switched to OFF Mode it is also OFF in Sleep Mode)

Table 11 CAN Modes change when switching to SBC Sleep Mode

Programmed CAN Mode in SBC Normal Mode	CAN_x bits	SYSERR bit	CAN Mode in SBC Sleep Mode	CAN_x bits
CAN OFF	000	0	CAN OFF	000
CAN WK Mode (no SWK)	001	0	CAN WK Mode (no SWK)	001
CAN Receive Only (no SWK)	010	0	CAN WK Mode (no SWK)	001
CAN Normal Mode (no SWK)	011	0	CAN WK Mode (no SWK)	001
CAN OFF	100	0	CAN OFF	100
CAN SWK Mode	101	0	CAN SWK Mode	101
CAN SWK Mode	101	1	CAN WK Mode (no SWK)	101
CAN Receive Only with SWK	110	0	CAN SWK Mode	101
CAN Receive Only with SWK	110	1	CAN WK Mode (no SWK)	101

CAN Normal Mode with SWK	111	0	CAN SWK Mode	101
CAN Normal Mode with SWK	111	1	CAN WK Mode (no SWK)	101

5.4.4.4 SBC Restart Mode with SWK

If SBC Restart Mode is entered the transceiver can change the CAN mode. During Restart or after Restart the following modes are possible

- CAN OFF
- CAN WK Mode (either still wake cable or already woken up)
- CAN SWK Mode (WUF Wake from Sleep)

Table 12 CAN Modes change in case of Restart out of SBC Normal Mode

Programmed CAN Mode in SBC Normal Mode	CAN_x bits	SYSERR bit	CAN Mode in and after SBC Restart Mode	CAN_x bits	SYSERR bit
CAN OFF	000	0	CAN OFF	000	0
CAN WK Mode (no SWK)	001	0	CAN WK Mode (no SWK)	001	0
CAN Receive Only (no SWK)	010	0	CAN WK Mode (no SWK)	001	0
CAN Normal Mode (no SWK)	011	0	CAN WK Mode (no SWK)	001	0
CAN OFF	100	0	CAN OFF	100	0
CAN SWK Mode	101	0	CAN WK Mode (no SWK)	101	1
CAN SWK Mode	101	1	CAN WK Mode (no SWK)	101	1
CAN Receive Only with SWK	110	0	CAN WK Mode (no SWK)	101	1
CAN Receive Only with SWK	110	1	CAN WK Mode (no SWK)	101	1
CAN Normal Mode with SWK	111	0	CAN WK Mode (no SWK)	101	1
CAN Normal Mode with SWK	111	1	CAN WK Mode (no SWK)	101	1

The various reasons for entering SBC Restart Mode and the respective status flag settings are shown in **Table 13**.

Table 13 CAN Modes change in case of Restart out of SBC Sleep Mode

CAN Mode in SBC Sleep Mode	CAN Mode in and after SBC Restart Mode	CAN_x	SYS ERR	CAN_WU	WUP	WUF	ECNT_x	Reason for Restart
CAN OFF	CAN OFF	000	0	0	0	0	0	Wake on other wake source
CAN WK Mode	CAN woken up	001	0	1	1	0	0	Wake (WUP) on CAN
CAN WK Mode	CAN WK Mode	001	0	0	0	0	0	Wake on other wake source
CAN SWK Mode	CAN woken up	101	0	1	0/1[1)]	1	x	Wake (WUF) on CAN
CAN SWK Mode,	CAN woken up	101	1	1	0/1[2)]	0	100000	Wake due to error counter overflow
CAN SWK selected, CAN WK active	CAN woken up.	101	1	1	1	0	0	Wake (WUP) on CAN, config check was not pass
CAN SWK Mode	CAN WK Mode	101	1	0	0/1	0	x	Wake on other wake source

- In case there is a WUF detection within $t_{SILENCE}$ then the WUP bit will not be set. Otherwise it will always be set together with the WUF bit.

- In some cases the WUP bit might stay cleared even after $t_{SILENCE}$, e.g. when the error counter expires without detecting a wake up pattern.

5.4.4.5 SBC Fail-Safe Mode with SWK

When SBC Fail-Safe Mode is entered the CAN transceiver is automatically set into WK Mode (wake capable) without the selective wake function.

5.4.5 Wake-up

A wake-up via CAN leads to a restart out of SBC Sleep Mode and to an interrupt in SBC Normal Mode, and in SBC Stop Mode. After the wake event the bit CAN_WU is set, and the details about the wake can be read out of the bits WUP, WUF,SYSERR, and ECNT.

5.4.6 Configuration for SWK

The CAN protocol handler settings can be configured in following registers:

- **SWK_BTL1_CTRL** defines the number of time quanta in a bit time. This number depends also on the internal clock settings performed in the register **SWK_CDR_CTRL2**;
- **SWK_BTL2_CTRL** defines the sampling point position;
- The respective receiver during frame detection mode can be selected via the bit **RX_WK_ SEL**;
- The clock and data recovery (see also **Chapter 5.4.8**) can be configured in the registers **SWK_CDR_CTRL1**, **SWK_CDR_CTRL2**, **SWK_CDR_LIMIT_HIGH_CTRL** and **SWK_CDR_LIMIT_LOW_CTRL**;

The actual configuration for selective wake is done via the Selective Wake Control Registers SWK_IDx_CTRL, SWK_MASK_IDx_CTRL, SWK_DLC_CTRL, SWK_DATAx_CTRL.

The oscillator has the option to be trimmed by the microcontroller. To measure the oscillator, the SPI bit OSC_CAL needs to be set to 1 and a defined pulse needs to be given to the TXDCAN pin by the microcontroller (e.g. 1µs pulse, CAN needs to be switched off before). The SBC measures the length of the pulse by counting the time with the integrated oscillator. The counter value can be read out of the register SWK_OSC_CAL H_STATE and SWK_OSC_CAL_L_STATE. To change the oscillator the trimming function needs to be enabled by setting the bits TRIM_EN_x = 11 (and OSC_CAL = 1). The oscillator can then be adjusted by writing into the registers **SWK_OSC_TRIM_CTRL** and **SWK_OPT_CTRL**. To finish the trimming, the bits TRIM_EN_x need to be set back to “00”.

5.4.7 CAN Flexible Data Rate (CAN FD) Tolerant Mode

The CAN FD tolerant mode can be activated by setting the bit **CAN_FD_ EN**= ‘1’ in the register **SWK_CAN_FD_CTRL**. With this mode the internal CAN frame decoding will be stopped for CAN FD frame formats:

- The high baudrate part of a CAN FD frame will be ignored,
- No Error Handling (Bit Stuffing, CRC checking, Form Errors) will be applied to remaining CAN frame fields (Data Field, CRC Field, …),
- No wake up is done on CAN FD frames.

The internal CAN frame decoder will be ready for new CAN frame reception when the End of frame (EOF) of a CAN FD frame is detected.The identification for a CAN FD frame is based on the FDF Bit, which is sent in the Control Field of a CAN FD frame:

- FDF Bit = 1 identifies the current frame as an CAN FD frame and will stop further decoding on it.
- FDF Bit = 0 identifies the current frame as CAN 2.0 frame and processing of the frame will be continued.

In this way it is possible to send mixed CAN frame formats without affecting the selective wake functionality by error counter increment and subsequent misleading wake up. In addition to the **CAN_FD_ EN** bit also a filter setting must be provided for the CAN FD tolerant mode. This filter setting defines the minimum dominant time for a CAN FD dominant bit which will be considered as a dominant bit from the CAN FD frame decoder. This value must be aligned with the selected high baudrate of the data field in the CAN network.

To support programming via CAN during CAN FD mode a dedicated SPI bit **DIS_ERR_ CNT** is available to avoid an overflow of the implemented error counter (see also **Chapter 5.4.2.4**).

The behavior of the error counter depends on the setting of the bits **DIS_ERR_ CNT** and **CAN_FD_ EN** and is show in below table:

Table 14 Error Counter Behavior

DIS_ERR_ CNT setting	CAN_FD_ EN setting	Error Counter Behavior
0	0	Error Counter counts up when a CAN FD frame or an incorrect/corrupted CAN frame is received; counts down when a CAN frame is received properly (as specified in ISO 11898-2:2016)
1	0	Error Counter counts up when a CAN FD frame or an incorrect/corrupted CAN frame is received; counts down when a CAN frame is received properly (as specified in ISO 11898-2:2016)
0	1	Error Counter counts down when correct CAN (incl. CAN FD) frame is received
1	1	Error Counter is and stays cleared to avoid an overflow during programming via CAN

The **DIS_ERR_ CNT** bit is automatically cleared at Tsilence ($t_{SILENCE}$) expiration.

5.4.8 Clock and Data Recovery

In order to compensate possible deviations on the CAN oscillator frequency caused by assembly and lifetime effects, the device features an integrated clock and data recovery (CDR).

It is recommended to always enable the CDR feature during SWK operation.

5.4.8.1 Configuring the Clock Data Recovery for SWK

The Clock and Data Recovery can be optionally enabled or disabled with the **CDR_EN** bit in the **SWK_CDR_CTRL1** SPI register. In case the feature is enabled, the CAN bit stream will be measured and the internal clock used for the CAN frame decoding will be updated accordingly.
Before the Clock and Data Recovery can be used it must be configured properly related to the used baud rate and filtering characteristics (see **Chapter 5.4.8.2**).

It is strongly recommended not to enable/disable the Clock Recovery during a active CAN Communication. To ensure this, it is recommended to enable/disable it during CAN OFF (**BUS_CTRL_1**; CAN[2:0] = 000).

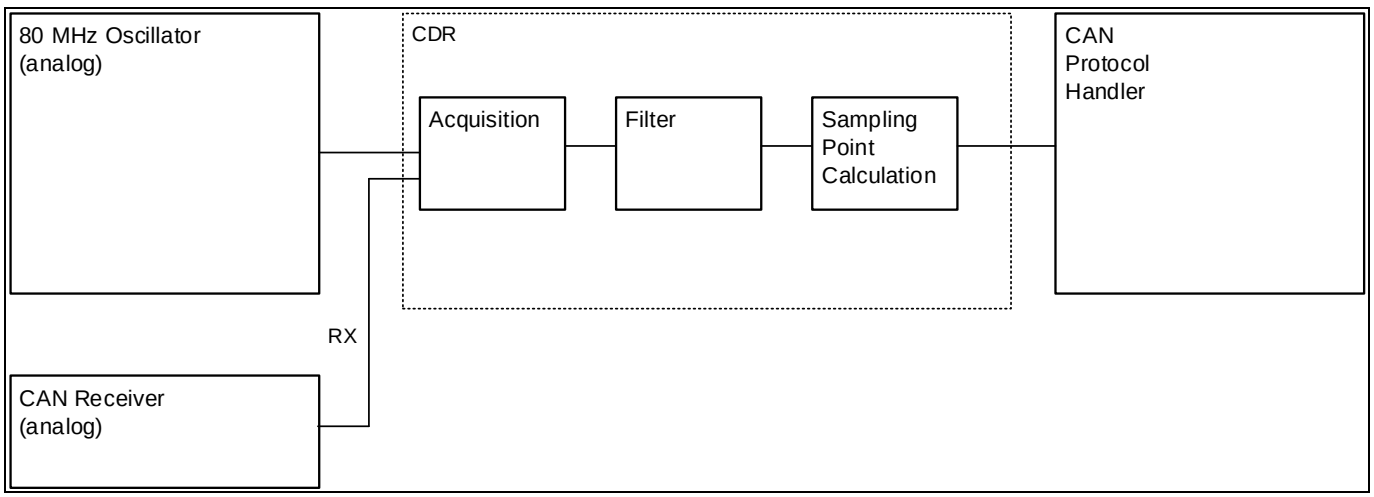


Figure 15 Clock and Data Recovery Block Diagram

5.4.8.2 Setup of Clock and Data Recovery

It is strongly recommended to enable the clock and data recovery feature only when the setup of the clock and data recovery is finished.
The following sequence should be followed for enabling the clock and data recovery feature:

- Step 1: Switch CAN to OFF and **CDR_EN** to OFF
  Write SPI Register BUS_CTRL_1 (CAN[2:0] = 000).
- Step 2: Configure CDR Input clock frequency
  Write SPI Register **SWK_CDR_CTRL2** (SEL_OSC_CLK[1:0]).
- Step 3: Configure Bit timing Logic
  Write SPI Register **SWK_BTL1_CTRL** and adjust **SWK_CDR_LIMIT_HIGH_CTRL** and **SWK_CDR_LIMIT_LOW_CTRL** according to **Table 38**.
- Step 4: Enable Clock and Data Recovery
  Choose filter settings for Clock and Data recovery. Write SPI Register **SWK_CDR_CTRL1** with **CDR_EN** = 1

Additional hints for the CDR configuration and operation:

- Even if the CDR is disabled, when the baud rate is changed, the settings of **SEL_OSC_CLK** in the register **SWK_CDR_CTRL1** and **SWK_BTL1_CTRL** have to be updated accordingly,
- The **SWK_CDR_LIMIT_HIGH_CTRL** and **SWK_CDR_LIMIT_LOW_CTRL** registers have to be also updated when the baud rate or clock frequency is changed (the CDR is discarding all the acquisitions and looses all acquired information, if the limits are reached -the **SWK_BTL1_CTRL** value is reloaded as starting point for the next acquisitions)
- When updating the CDR registers, it is recommended to disable the CDR and to enable it again only after the new settings are updated,
- The **SWK_BTL2_CTRL** register represents the sampling point position. It is recommended to be used at default value: 11 0011 (~80%)

5.4.9 Electrical Characteristics

Table 15 Electrical Characteristics

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; 4.75 V < VCAN < 5.25 V; RL = 60Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			
CAN Partial Network Timing							
Timeout for bus inactivity	$t_{SILENCE}$	0.6	–	1.2	s	1)	
Bias reaction time	t_{bias}	–	–	200	µs	1)Load R_L = 60 Ω, C_L = 100 pF, C_{GND} = 100 p	
Wake-up reaction time (WUP or WUF)	$T_{WU\_WUP/WUF}$	–	–	100	µs	1)2)3) Wake-up reaction time after a valid WUP or WUF;	
Min. Bit Time	t_{Bit_min}	1	–	–	µs	1)4)	
CAN FD Tolerance[5)]							
SOF acceptance	n_{Bits_idle}	6	–	10	bits	6) Number of recessive bits before a new SOF shall be accepted	
Dominant signals which are ignored (up to 2MBit/s)	$t_{FD\_Glitch\_4}$	0	–	5	%	6)7)of arbitration bit time; to be configured via **FD_FILTER**;	

Dominant signals which are ignored (up to 5MBit/s)	$t_{FD\_Glitch\_10}$	0	–	2.5	%	6)8)of arbitration bit time; to be configured via **FD_FILTER**;	
Signals which are detected as a dominant data bit after the FDF bit and before EOF bit (up to 2MBit/s)	$t_{FD\_DOM\_4}$	17.5	–	–	%	6)7)of arbitration bit time; to be configured via **FD_FILTER**;	
Signals which are detected as a dominant data bit after the FDF bit and before EOF bit (up to 5MBit/s)	$t_{FD\_DOM\_10}$	8.75	–	–	%	6)8)of arbitration bit time; to be configured via **FD_FILTER**;	

1) Not subject to production test, tolerance defined by internal oscillator tolerance
2) Wake-up signalized via INT pin activation in SBC Stop Mode and via VCC1 ramping up with wake from SBC Sleep Mode.
3) WUP: time starts with end of last dominant phase of WUP; WUF: time starts with end of CRC delimiter of the WUF.
4) The minimum bit time corresponds to a maximum bit rate of 1 Mbit/s. The lower end of the bit rate depends on the protocol IC or the permanent dominant detection circuitry preventing a permanently dominant clamped bus.
5) Applies for an arbitration rate of up to 500kbps until the FDF bit is detected and **RX_WK_ SEL** = 0.
6) Not subject to production test; specified by design.
7) A data phase bit rate less or equal to four times of the arbitration bit rate or 2 Mbit/s, whichever is lower.
8) A data phase bit rate less or equal to ten times of the arbitration bit rate or 5 Mbit/s, whichever is lower.

6 Voltage Regulator 1

6.1 Block Description

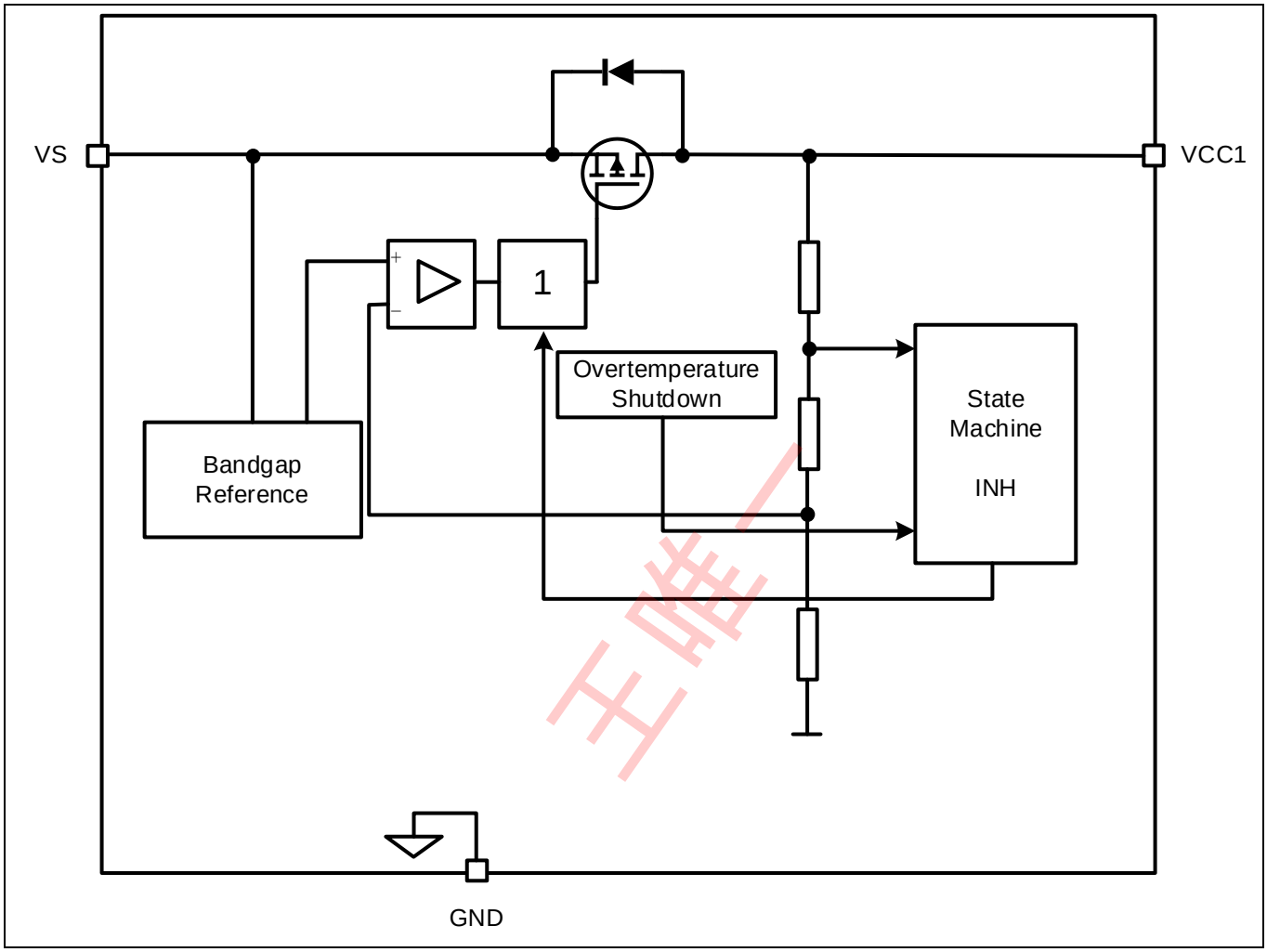


Figure 16 Module Block Diagram

Functional Features

- 5V / 3.3V low-drop voltage regulator.
- Undervoltage monitoring with adjustable reset level, VCC1 prewarning and VCC1 short circuit detection ($V_{RT1/2/3/4}$,$V_{PW,f}$). Please refer to **Chapter 15.6** and **Chapter 15.7** for more information.
- Short circuit detection and switch off with undervoltage fail threshold, device enters SBC Fail-Safe Mode
- ≥470nF ceramic capacitor at voltage output for stability, with ESR < 1Ω @ f = 10 kHz,to achieve the voltage regulator control loop stability based on the safe phase margin (bode diagram).
- Output current capability up to $I_{VCC1,lim}$.

6.2 Functional Description

Voltage Regulator 1 (VCC1) is enabled in SBC Normal and SBC Stop modes, and disabled in SBC Sleep and SBC Fail-Safe modes. The regulator is capable of supplying an output current up to $I_{VCC1,lim}$.

To minimize quiescent current in SBC Stop mode, only the low-power regulator—characterized by lower accuracy ($V_{CC1,out41}$)—remains active for small load conditions, resulting in decreased output voltage tolerance. When the load current on VCC1 exceeds the selected active peak threshold ($I_{VCC1,Ipeak1,r}$ or $I_{VCC1,Ipeak2,r}$), the high-power regulator is automatically activated to optimize dynamic load response, causing a typical increase in current consumption of approximately 2.9 mA.

If the load current on VCC1 drops below the selected threshold ($I_{VCC1,Ipeak1,f}$ or $I_{VCC1,Ipeak2,f}$), the high-power regulator is disabled and the device reverts to low-quiescent current mode.

In SBC Normal mode, both the low-power and high-power regulators operate simultaneously.

Two selectable active peak thresholds are available via SPI:

- **I_PEAK_TH** = '0' (default): Lower VCC1 active peak threshold 1 is selected, providing the lowest quiescent current consumption in SBC Stop mode ($I_{Stop\_1,25}$, $I_{Stop\_1,85}$).
- **I_PEAK_TH** = '1': Higher VCC1 active peak threshold 2 is selected, resulting in increased quiescent current consumption in SBC Stop mode ($I_{Stop\_2,25}$, $I_{Stop\_2,85}$).

6.3 Electrical Characteristics

Table 16 Electrical Characteristics

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			
Output Voltage including line and Load regulation	$V_{CC1,out1}$(5V)	4.9	5.0	5.1	V	1)SBC Normal Mode; 10µA < I_{VCC1} < 250mA 6V < V_S < 28V	
	$V_{CC1,out1}$(3V3)	3.23	3.3	3.37			
Output Voltage including line and Load regulation	$V_{CC1,out2}$(5V)	4.9	5.0	5.1	V	1)SBC Normal Mode; 10µA < I_{VCC1} < 150mA	
	$V_{CC1,out2}$(3V3)	3.23	3.3	3.37			
Output Voltage including line and Load regulation	$V_{CC1,out3}$(5V)	4.95	-	5.05	V	1)2)SBC Normal Mode; 20mA < I_{VCC1} < 90mA 8V < V_S < 18V 25°C < T_j < 125°C	
	$V_{CC1,out3}$(3V3)	3.27	-	3.34			
Output Voltage including line and Load regulation	$V_{CC1,out41}$(5V)	4.8	-	5.2	V	SBC Stop Mode; 1mA < I_{VCC1} < $I_{VCC1,Ipeak}$	
	$V_{CC1,out41}$(3V3)	3.26	-	3.4			
Output Voltage including line and Load regulation	$V_{CC1,out42}$(5V)	4.8	-	5.2	V	SBC Stop Mode; 10µA < I_{VCC1} < 1mA	
	$V_{CC1,out42}$(3V3)	3.26	-	3.4			
Output Drop	$V_{CC1,d2}$	–	–	500	mV	I_{VCC1} = 150mA V_S=5V	
VCC1 Active Peak Threshold 1 (Transition threshold between low-power and high- power mode regulator)	$I_{VCC1,Ipeak1,r}$	–	2.9	5.5	mA	2) I_{CC1} rising; V_S = 13.5V -40°C < T_j < 150°C; **I_PEAK_TH** = '0'	
VCC1 Active Peak Threshold 1 (Transition threshold between high-power and low- power mode regulator)	$I_{VCC1,Ipeak1,f}$	0.5	2.2	–	mA	2) I_{CC1} falling; V_S = 13.5V -40°C < T_j < 150°C; **I_PEAK_TH** = '0'	
VCC1 Active Peak Threshold 2 (Transition threshold between low-power and high- power mode regulator)	$I_{VCC1,Ipeak2,r}$	–	5.5	9.0	mA	2) I_{CC1} rising; V_S = 13.5V -40°C < T_j < 150°C; **I_PEAK_TH** = '1'	
VCC1 Active Peak Threshold 2 (Transition threshold	$I_{VCC1,Ipeak2,f}$	1.7	4.5	–	mA	2) I_{CC1} falling; V_S = 13.5V -40°C < T_j < 150°C; **I_PEAK_TH** = '1'	

between high-power and low- power mode regulator)							
Overcurrent Limitation	$I_{VCC1,lim}$	250	–	1200[2]	mA	current flowing out of pin, V_{CC1} = 0V	

1) In SBC Stop Mode, the specified output voltage tolerance applies when I_{VCC1} has exceeded the selected active peak threshold ($I_{VCC1,Ipeak1,r}$ or $I_{VCC1,Ipeak2,r}$) but with increased current consumption.
2) Not subject to production test, specified by design.

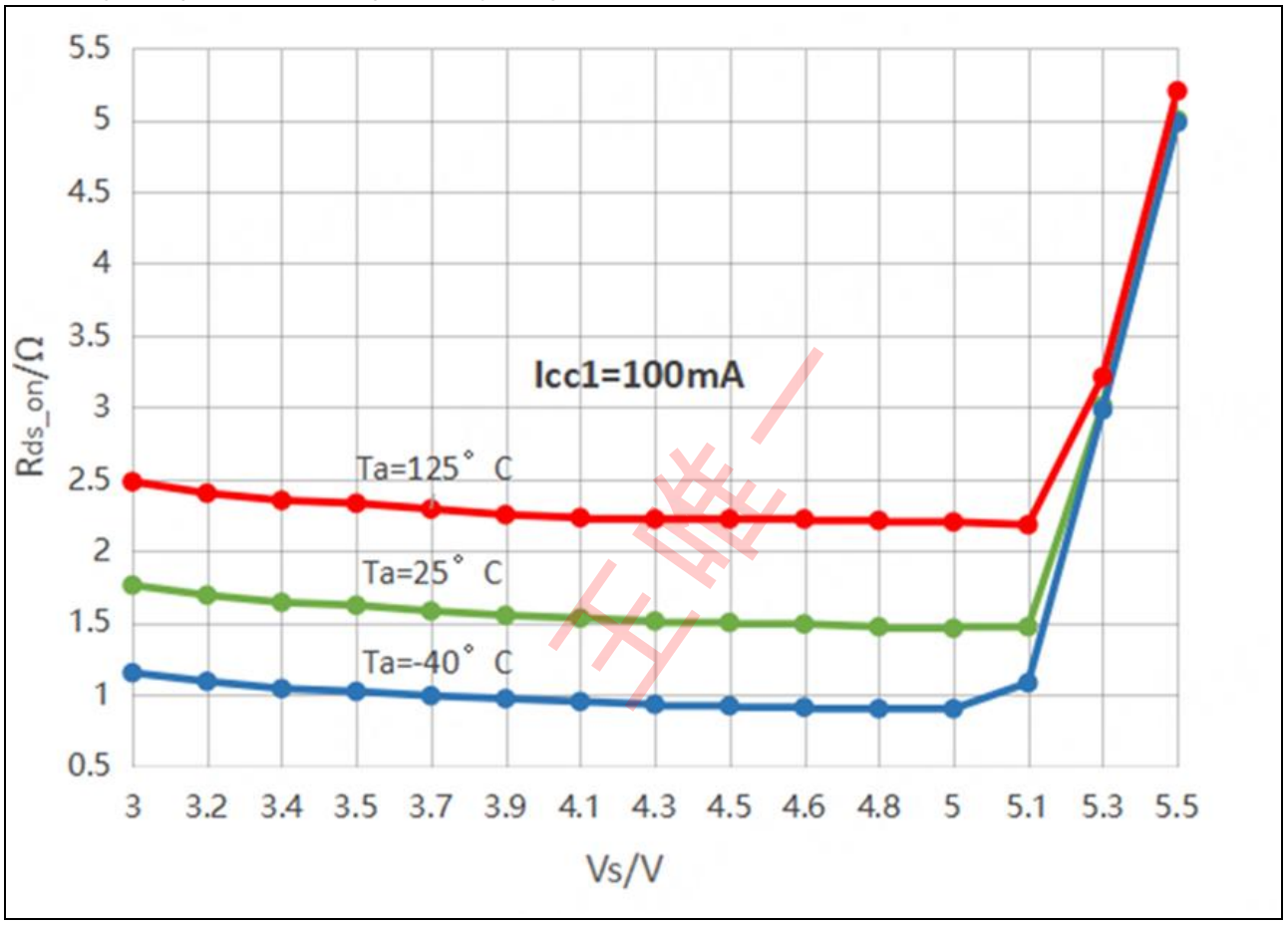


Figure 17 Typical on-resistance of VCC1 (5V) pass device during low drop operation for I_{CC1} = 100mA

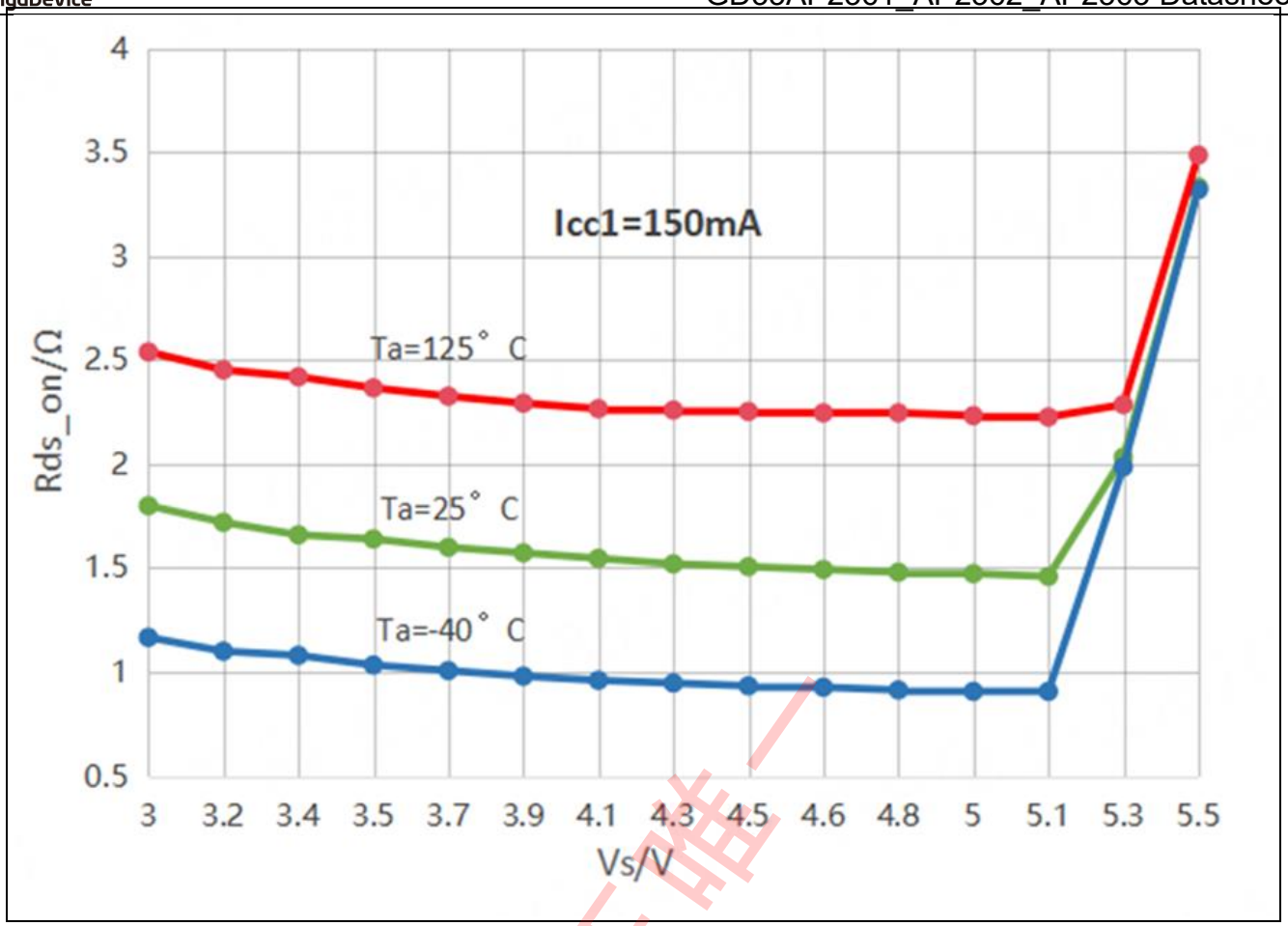


Figure 18 Typical On-resistance range of VCC1(5V) pass device during low drop operation for I_{CC1} = 150mA

7 Voltage Regulator 2

7.1 Block Description

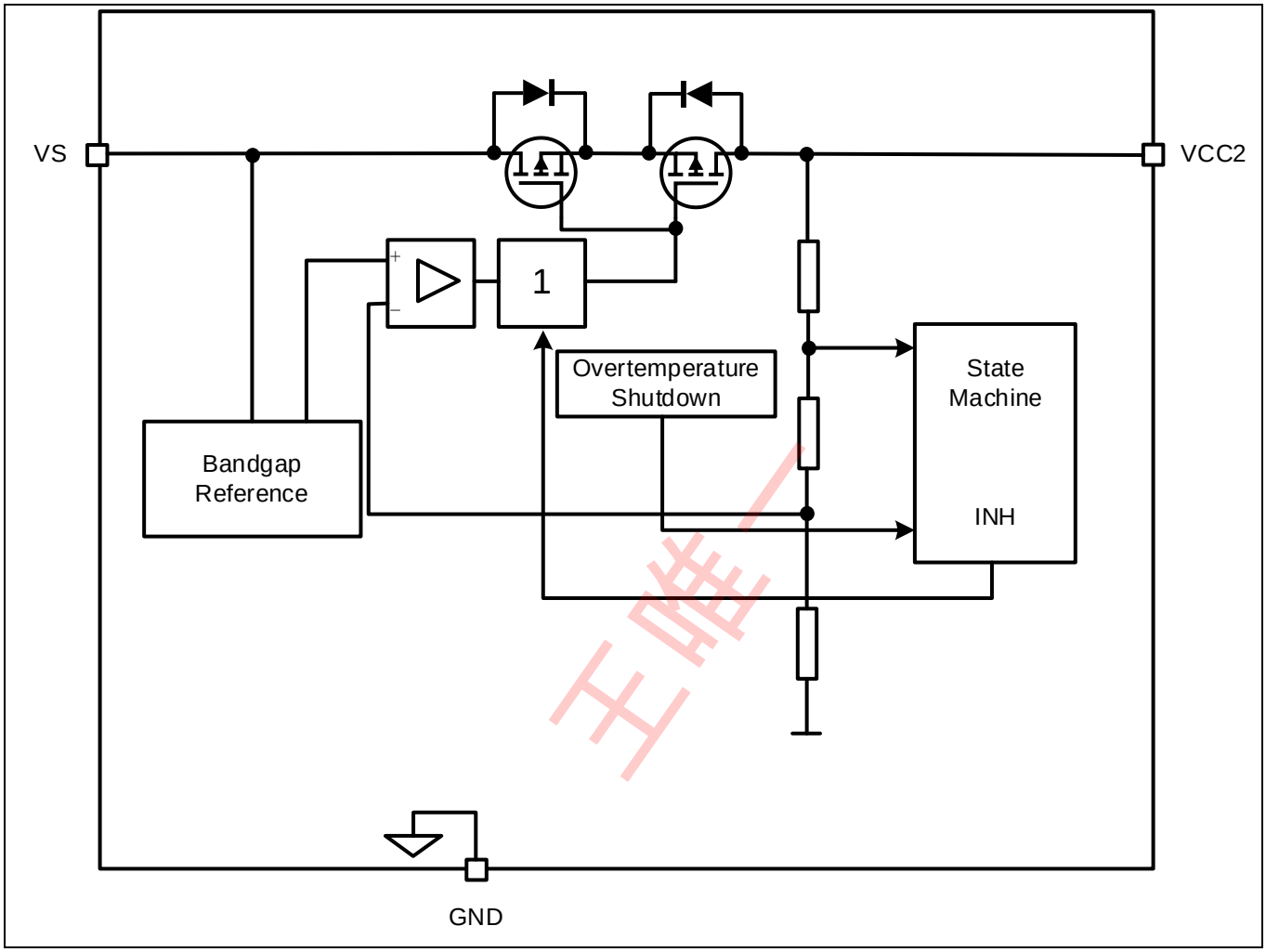


Figure 19 Module Block Diagram

Functional Features

- 5 V low-drop voltage regulator
- Protected against short to battery voltage, e.g. for off-board sensor supply
- Can also be used for CAN supply
- VCC2 over-/under-voltage monitoring. Please refer to **Chapter 15.8** for more information
- Can be active in SBC Normal, SBC Stop, and SBC Sleep Mode (not SBC Fail-Safe Mode)
- VCC2 switch off after entering SBC Restart Mode. Switch off is latched, LDO must be enabled via SPI after shutdown.
- Overtemperature protection
- ≥ 470nF ceramic capacitor at output voltage for stability, with ESR < 1Ω @ f = 10 kHz,to achieve the voltage regulator control loop stability based on the safe phase margin (bode diagram).
- Output current capability up to $I_{VCC2,lim}$.

7.2 Functional Description

In SBC Normal Mode, VCC2 is controlled via SPI. For SBC Stop or Sleep modes, the VCC2 state must be configured prior to entering the respective mode. The regulator can deliver an output current up to $I_{VCC2,lim}$.

To minimize quiescent current in SBC Stop Mode, a low-power regulator with reduced accuracy ($V_{CC2,out5}$) services light loads, which results in a relaxed output voltage tolerance. If the VCC2 load current exceeds the turn-on threshold ($I_{VCC2} > I_{VCC2,Ipeak,r}$), the high-power regulator is enabled to improve dynamic load response, causing a typical increase in device current of approximately 2.9 mA. When the load current falls below the turn-off threshold ($I_{VCC2} < I_{VCC2,Ipeak,f}$), the high-power regulator is disabled and the low-quiescent mode is resumed. Both regulators operate concurrently in SBC Normal Mode.

Note: If VCC2 supplies external (off-board) loads, the application must take into account the series resonance formed by cable inductance and the load decoupling capacitor. Adequate damping is required to ensure stable operation.

7.2.1 Short to Battery Protection

The output stage is protected for short to VBAT.

7.3 Electrical Characteristics

Table 17 Electrical Characteristics

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			
Output Voltage including line and Load regulation (SBC Normal Mode)	$V_{CC2,out1}$	4.9	5.0	5.1	V	1)SBC Normal Mode; 10µA < I_{VCC2} < 100mA 6.5V < V_S < 28V	
Output Voltage including line and Load regulation (SBC Normal Mode)	$V_{CC2,out2}$	4.9	5.0	5.1	V	1)SBC Normal Mode; 10µA < I_{VCC2} < 80mA 6V < V_S < 28V	
Output Voltage including line and Load regulation (SBC Normal Mode)	$V_{CC2,out3}$	4.9	5.0	5.1	V	1)SBC Normal Mode; 10µA < I_{VCC2} < 40mA	
Output Voltage including line and Load regulation (SBC Normal Mode)	$V_{CC2,out4}$	4.95	–	5.05	V	2)SBC Normal Mode; 10µA < I_{VCC2} < 5mA 8V < V_S < 18V 25°C < T_j < 125°C	
Output Voltage including line and Load regulation (SBC Stop/Sleep Mode)	$V_{CC2,out5}$	4.8	–	5.2	V	Stop, Sleep Mode; 1mA < I_{VCC2} < $I_{VCC2,Ipeak}$	
Output Voltage including line and Load regulation (SBC Stop/Sleep Mode)	$V_{CC2,out6}$	4.8	–	5.2	V	Stop, Sleep Mode; 10µA < I_{VCC2} < 1mA	
Output Drop	$V_{CC2,d1}$	–	–	500	mV	I_{VCC2} = 30mA V_S = 5V	
VCC2 Active Peak Threshold (Transition threshold between low-power and high-power mode regulator)	$I_{VCC2,Ipeak,r}$	–	2.9	5.5	mA	2)I_{CC2} rising; V_S = 13.5V -40°C < T_j < 150°C	

VCC2 Active Peak Threshold (Transition threshold between high-power and low-power mode regulator)	$I_{VCC2,Ipeak,f}$	0.5	2.4	–	mA	2)I_{CC2} falling; V_S = 13.5V -40°C < T_j < 150°C	
Overcurrent limitation	$I_{VCC2,lim}$	100	–	750[2)]	mA	current flowing out of pin, V_{CC2} = 0V	

1) In SBC Stop Mode, the specified output voltage tolerance applies when I_{VCC2} has exceeded the selected active peak threshold ($I_{VCC2,Ipeak,r}$) but with increased current consumption.
2) Not subject to production test, specified by design.

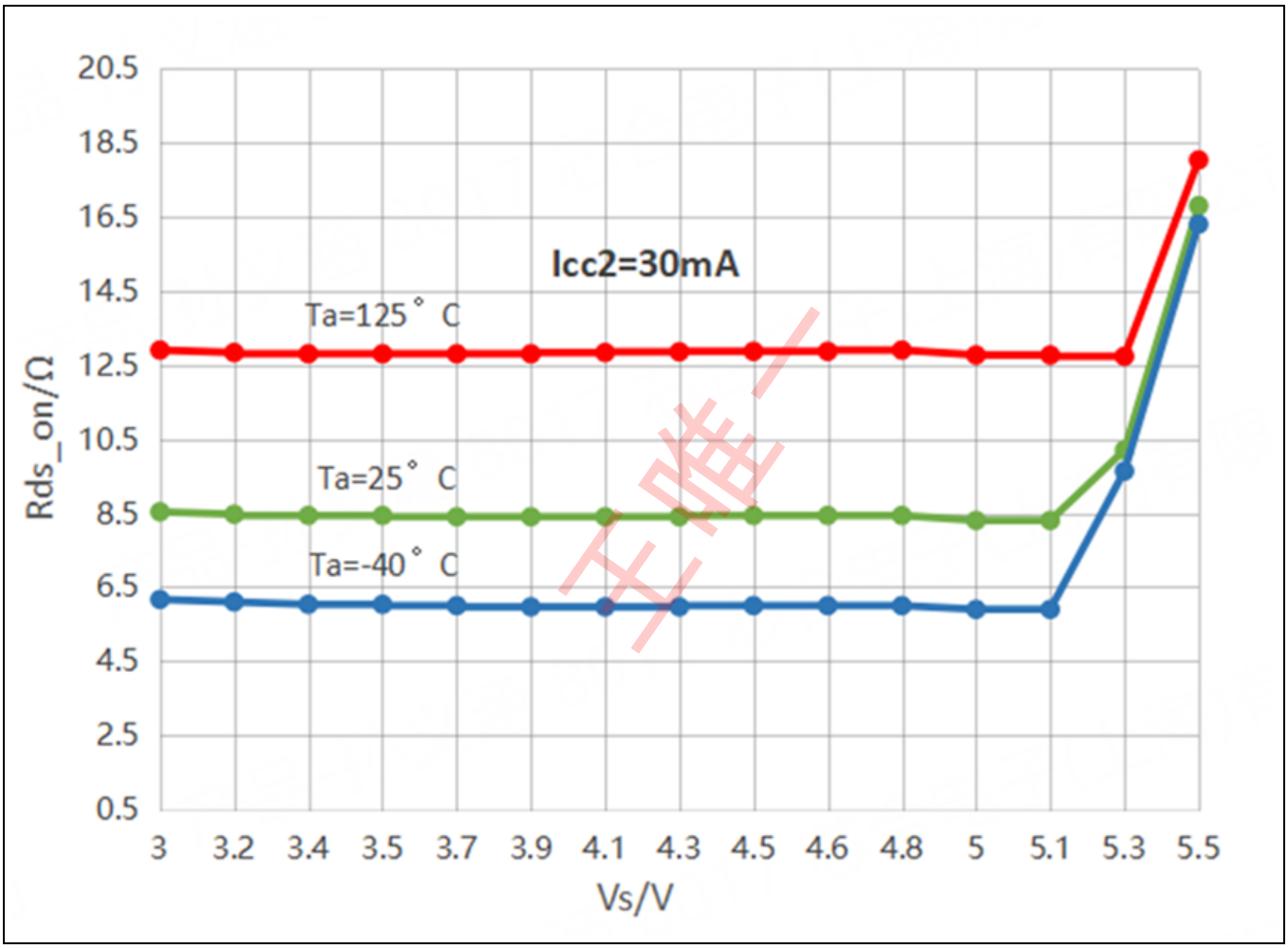


Figure 20 Typical on-resistance of VCC2 pass device during low drop operation for I_{CC2} = 30mA

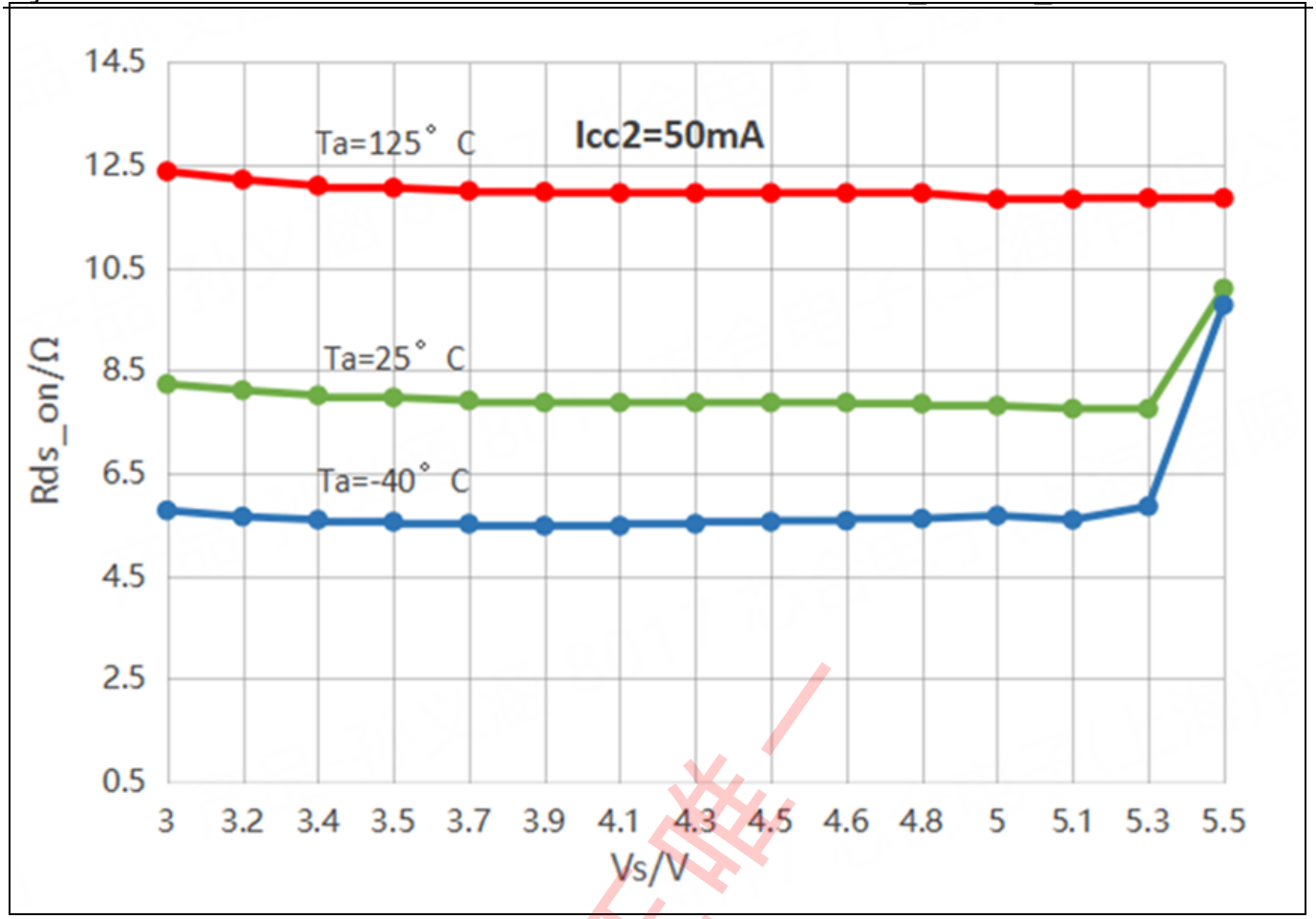


Figure 21 Typical On-resistance range of VCC2 pass device during low drop operation for I_{CC2} = 50mA

8 External Voltage Regulator 3

8.1 Block Description

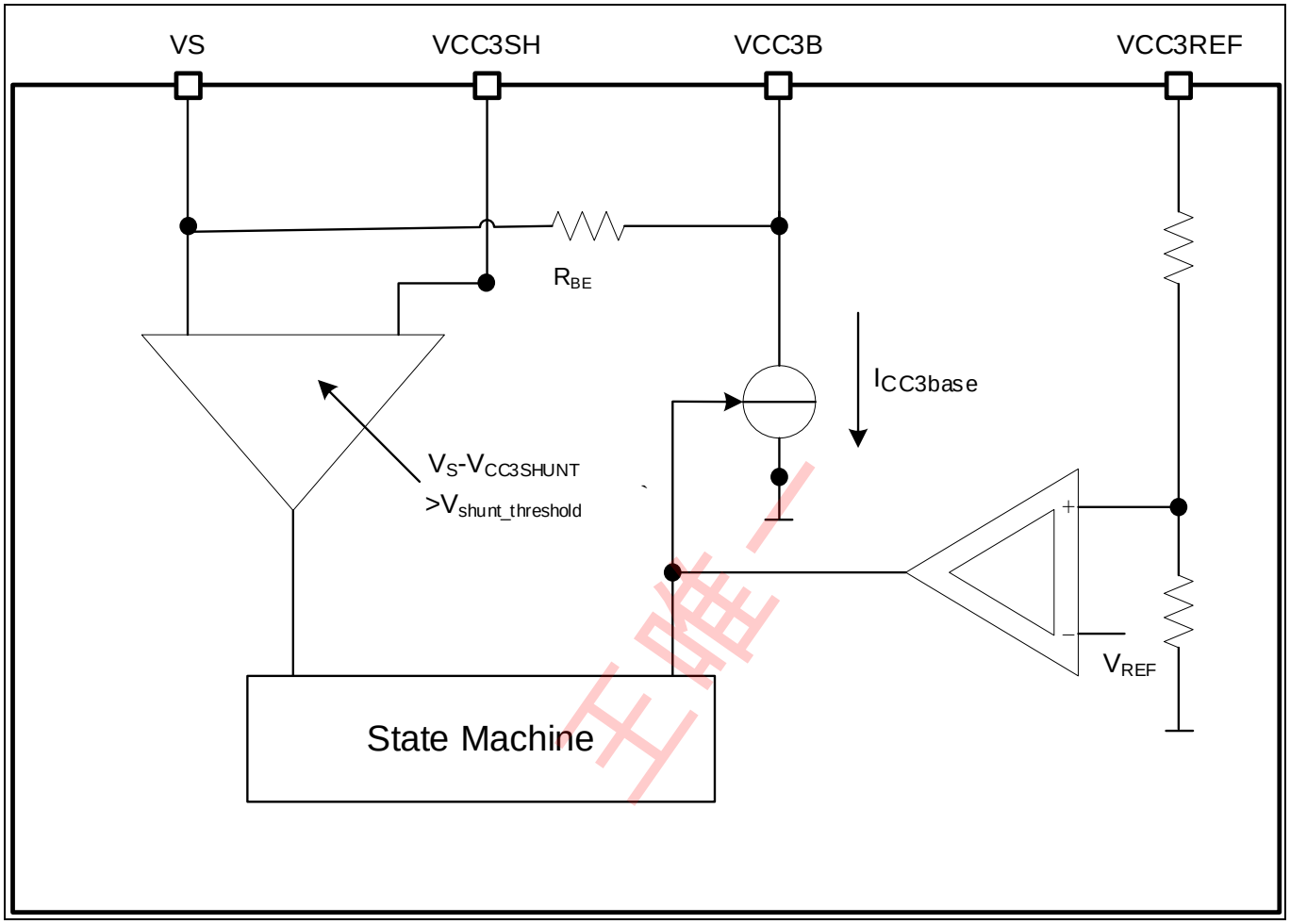


Figure 22 Functional Block Diagram

Functional Features

- Low-drop voltage regulator with external PNP transistor (up to 350mA with 470mΩ shunt resistor)
- Four high-voltage pins are used: VS,VCC3B,VCC3SH,VCC3REF
- Configurable as stand-alone regulator (5V/3.3V or 3.3V/1.8V output voltage selectable via SPI) or in load-sharing mode with VCC1 (5V or 3.3V output voltage)
- ≥ 4.7µF ceramic capacitor at output voltage for stability, with ESR < 150mΩ @ f = 10 kHz to achieve the voltage regulator control loop stability based on the safe phase margin (bode diagram).
- Overcurrent limitation with external shunt in stand-alone configuration
- Adjustable load current sharing ratio between VCC1 and VCC3 for load-sharing configuration
- Undervoltage shutdown in stand-alone configuration only

Table 18 [1)]External Voltage Regulator Configurations depending on VCC1 output voltage

VCC1 Version	VCC3 voltage for VCC3_V_CFG = 0	VCC3 voltage for VCC3_V_CFG = 1
VCC1 = 5.0V	VCC3 = 5.0V	VCC3 = 3.3V
VCC1 = 3.3V (V33 ver.)	VCC3 = 3.3V	VCC3 = 1.8V

1) This settings are valid only for the VCC3 stand-alone configuration. The bit **VCC3_V_CFG** is ignored for VCC3 load sharing configuration

8.2 Functional Description

The external voltage regulator can operate either as an independent regulator or in load-sharing mode with VCC1. In SBC Normal Mode, setting the **VCC3_ON** bit in the **M_S_CTRL** register configures VCC3 as a stand-alone voltage regulator. Alternatively, enabling the **VCC3_LS** bit in the **HW_CTRL** register via SPI activates the load-sharing configuration with VCC1.

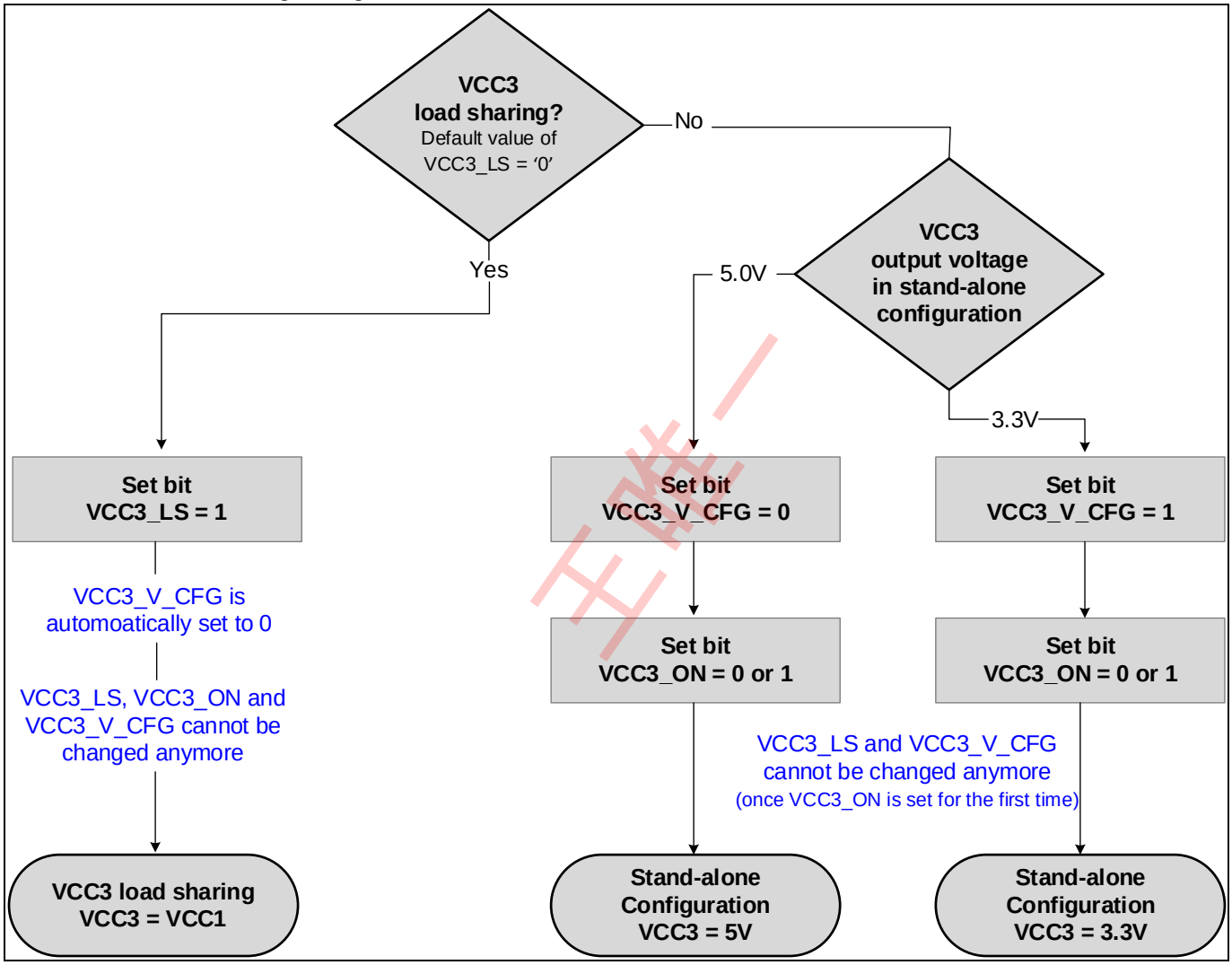


Figure 23 Example - Selecting the Configuration of the VCC3 Regulator (VCC1=5V)

Depending on the configuration, the external regulator operates according to the respective SBC mode as outlined in **Table 19**. Once the VCC3 configuration is selected, it cannot be modified.

In stand-alone mode, the maximum output current (**ICC3max**) is limited by the current restriction defined by the external shunt resistor. In load-sharing mode, the same shunt determines the current ratio between VCC1 and VCC3. Because the junction temperature of the external PNP transistor cannot be monitored by the SBC, thermal protection is not provided by the device and must be evaluated within the application design.

To minimize quiescent current in SBC Stop Mode, the output voltage tolerance is relaxed as only a low-power regulator with reduced accuracy remains active for small loads. When the base current on VCC3 exceeds the threshold (IVCC3base > IVCC3base,Ipeak,r), the high-power regulator is additionally enabled to support optimal dynamic load performance. Once the base current drops below (IVCC3base < IVCC3base,Ipeak,f), the device returns to low-quiescent operation by disabling the high-power regulator.

In SBC Normal Mode, only the high-power regulator is active.

The operational status of VCC3 is indicated in the **SUP_STAT_2** SPI register. The regulator switches OFF when the supply voltage (VS) falls below **VS_UV**, regardless of configuration, and automatically re-enables once VS exceeds the undervoltage threshold—unless the control bit **VCC3_VS_ UV_OFF** is set. To maintain VCC3 operation below the **VS_UV** threshold, this bit must be enabled. Additionally, when load-sharing mode is configured, VCC3 remains active in SBC Stop Mode if the **VCC3_LS_ STP_ON** bit is set.For detailed protection features, refer to **Chapter 15.7** and **Chapter 16.3**.

Table 19 External Voltage Regulator State by SBC Mode

SBC Mode	Load Sharing Mode[1)]	Independent Voltage Regulator
INIT Mode	OFF	OFF
Normal Mode	Configurable	Configurable
Stop Mode	OFF/Fixed[2)]	Fixed
Sleep Mode	OFF	Fixed
Restart Mode	ON or ramping	Fixed
Fail-Safe Mode	OFF	OFF

1) Behaves as VCC1 and has to be configured in SBC Normal Mode
2) Load Sharing operation in SBC Stop Mode is by default disabled for power saving reasons but **VCC3_LS** bit will stay set. However, it can be also configured via the SPI bit **VCC3_LS_ STP_ON** to stay enabled in SBC Stop Mode.

Notes

1. The configuration of the VCC3 voltage regulator must be performed immediately after device power-up and remains fixed as long as the device is powered.
2. Once either the **VCC3_ON** or **VCC3_LS** bit is set for the first time, the VCC3 configuration becomes permanent and cannot be modified. This configuration remains valid even after an SBC Soft Reset, provided the device continues to be supplied.
3. When VCC3 supplies external off-board loads, the application must account for the series resonance formed by the cable inductance and the decoupling capacitor at the load. Adequate damping must be ensured—for example, by placing a **100 Ω** resistor between the PNP collector and VCC3REF, together with a **10 µF** capacitor at the collector node (refer to **Figure 24**).

8.2.1 External Voltage Regulator as Independent Voltage Regulator

When configured as an independent voltage regulator, the SBC provides VCC3 as a third supply output that can be used as an off-board supply, for example to power sensors, through the integrated high-voltage pins VCC3B, VCC3SH, and VCC3REF.

This configuration is defined and latched by setting **VCC3_ON** = 1 while keeping **VCC3_LS** = 0. Once configured, VCC3 can be switched ON or OFF, but the configuration itself cannot be modified. Attempts to change the configuration do not trigger a **SPI_FAIL** error.

Overcurrent limitation is implemented via an external shunt resistor (refer to **Chapter 8.4** for shunt value calculation) and the corresponding shunt voltage threshold (**V shunt_threshold**). When this threshold is reached, the output current ICC3 is limited, and the **VCC3_OC** status bit is set. No additional protective reaction occurs, and the flag can be cleared via SPI once the overcurrent condition is removed. If the overcurrent limitation function is not required, the VCC3SH and VS pins should be connected together.

In this configuration, undervoltage monitoring of VCC3 is active. An undervoltage event is indicated by the **VCC3_UV/VCC3_OV** bit in the **SUP_STAT_2** SPI register.

VCC3 overvoltage detection is by default disabled. When VCC3_OV_EN is set to 1, VCC3 overvoltage detection is enabled and an overvoltage event of VCC3 will set the VCC3_OV flag.

Note: To avoid undesired current consumption increase of the device it must be ensured that VCC3 is not connected to VCC1 in this configuration.

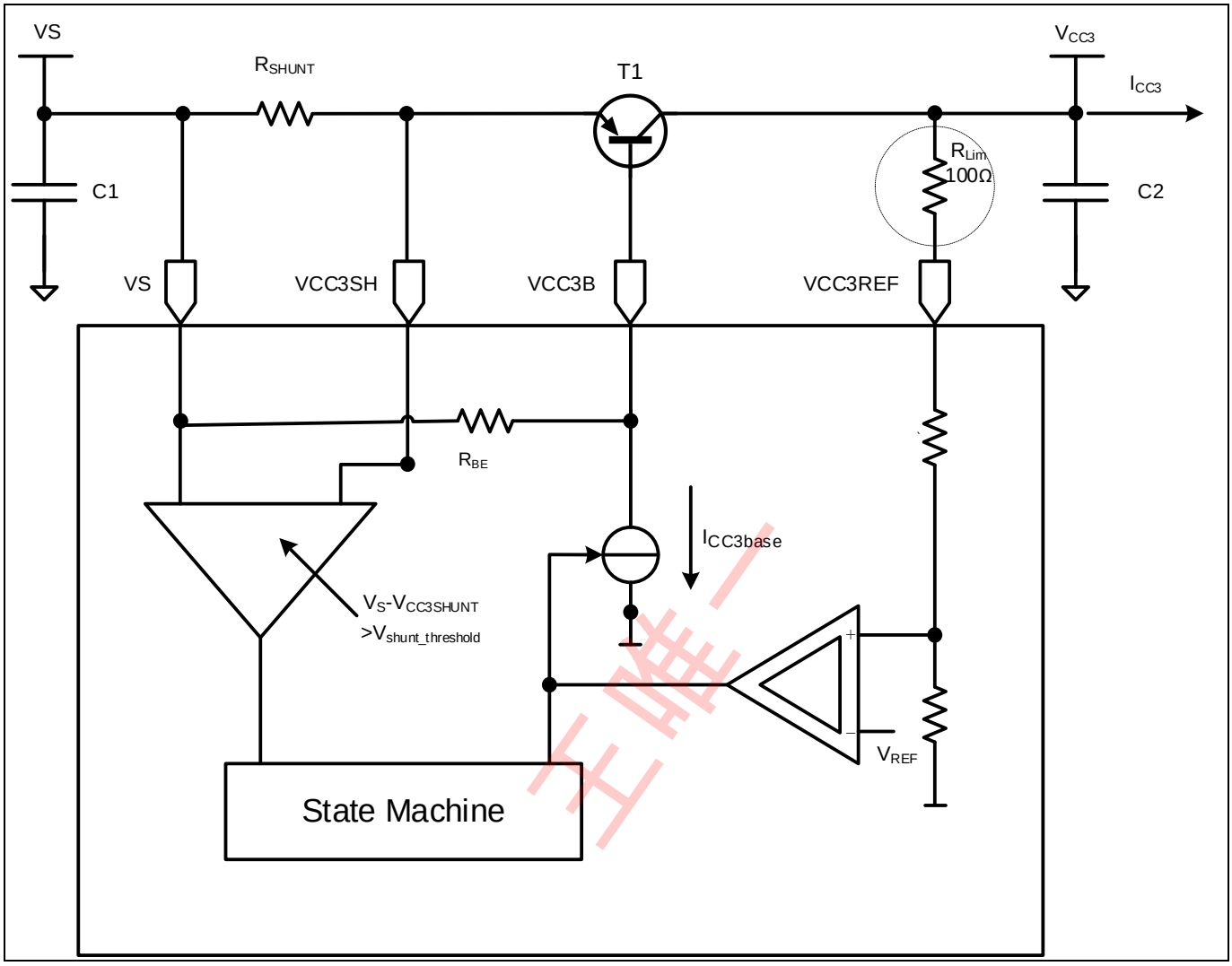


Figure 24 Protecting the VCC3 against inductive short circuits when configured as an independent voltage regulator for off-board supply

8.2.2 External Voltage Regulator in Load Sharing Mode

The purpose of the Load Sharing Mode is to increase the total current capability of VCC1 without adding additional power dissipation inside the SBC. In this mode, the load current is distributed between the internal VCC1 regulator and the external PNP transistor connected to VCC3. The typical setup for load sharing is shown in **Figure 25**. Load Sharing is active in SBC Normal Mode and can optionally be configured via SPI to remain active in SBC Stop Mode.

When used in load sharing configuration during SBC Normal Mode, an input voltage up to VSx,MAX is regulated to VCC3,nom = 5.0V (or 3.3 V for the V33 version) with a precision of ±2%.

This configuration is defined and latched by enabling **VCC3_LS = 1** for the first time while **VCC3_ON** remains inactive (**VCC3_ON = 0**). Once **VCC3_LS** has been set, any attempt to modify the VCC3 configuration will trigger the **SPI_FAIL** bit, leaving the configuration unchanged.

Load sharing is automatically disabled during SBC Stop Mode (only if **VCC3_LS_ STP_ON = 0**) for power-saving reasons; however, the configuration bit remains set, allowing automatic re-activation when the device returns to SBC Normal Mode. It must be ensured that the VCC3 output voltage level matches that of VCC1.

In this configuration, VCC3 does not provide undervoltage signalization. The VCC3 output is shut down when the device enters Fail-Safe Mode, for example due to an undervoltage event detected by VS_UV monitoring.

No overcurrent limitation is implemented in this mode; instead, the external shunt resistor defines the load sharing ratio between VCC1 and VCC3 currents (refer to **Equation (8.2)** in **Chapter 8.4**). Consequently, no **VCC3_OC** condition is reported in this configuration.

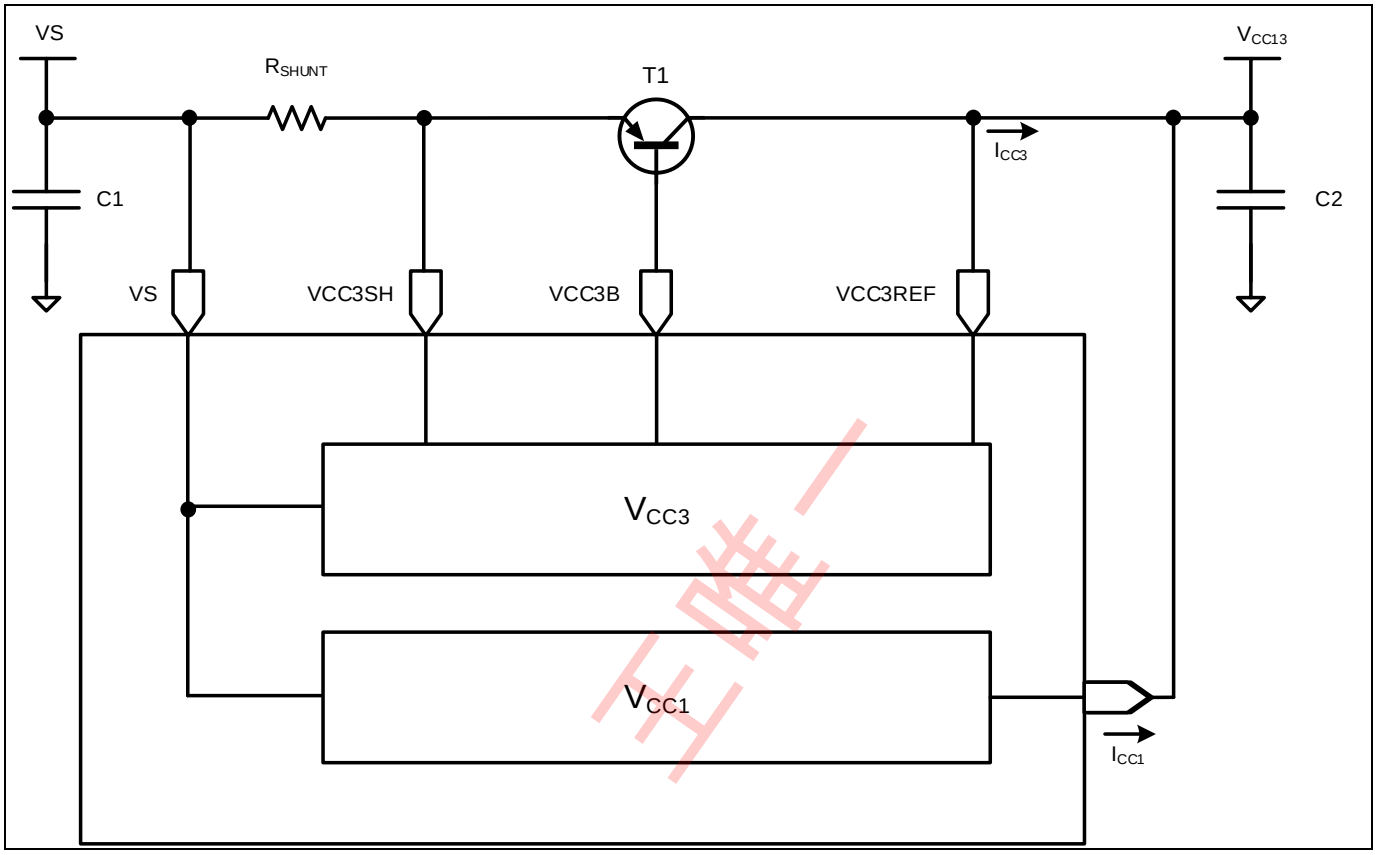


Figure 25 VCC3 in Load Sharing Configuration

8.3 External Components

Characterization has been performed using BCP52-16 (for ICC3 < 200 mA) and MJD253 transistors. Alternative PNP transistors may also be used; however, their functionality must be verified within the specific application.**Figure 25** illustrates one of the hardware setups used for characterization.

Table 20 Bill of Materials for the V_{CC3} Function with and without load sharing configuration

Device	Vendor	Reference / Value
C2	Murata	10 µF/10 V GCM31CR71A106K64L
RSHUNT	-	1 Ω (with / without LS)
T1	Infineon	BCP52-16

Note: The SBC does not provide thermal protection for the external PNP transistor. Therefore, the power-handling capability of the application must be selected according to the chosen PNP device, PCB layout, and system characteristics to avoid thermal damage. This can be achieved, for example, by implementing the shunt current limitation in the standalone configuration or by selecting an appropriate ICC1/ICC3 ratio in the load-sharing configuration.

Note: To ensure optimal EMC performance of the VCC3 regulator when the VCC3 output extends off-board, the PCB layout should be optimized to place the PNP transistor as close as possible to

the SBC. If this is not feasible or sufficient, an external capacitor should be added near the off-board connector (refer to **Chapter 17.1**).

8.4 Calculation of R_{SHUNT}

As a independent regulator, the maximum current I_{CC3max} where the limit starts and the bit $I_{CC3} > I_{CC3max}$ is set is determined by the shunt resistor R_{SHUNT} and the Output Current Shunt Voltage Threshold $V_{shunt\_threshold}$.
The resistor can be calculated as following:

$$R_{SHUNT} = \frac{U_{shunt_{threshold}}}{I_{CC3\max}} \quad (8.1)$$

If VCC3 is configured for load sharing, then the shunt resistor determines the load sharing ratio between VCC1 and VCC3. The ratio can be calculated as following:

$$\frac{I_{CC3}}{I_{CC1}} = \frac{\frac{110\Omega}{105} - \frac{15mV}{I_{CC1}}}{R_{SHUNT}} \quad (a) \quad (8.2)$$

$$I_{CC3} = \frac{I_{CC1} * 110\Omega/105 - 15mV}{R_{SHUNT}} \quad (b)$$

Example: A shunt resistor with 470mΩ and a load current of 100mA out of VCC1 would result in I_{CC3} = 191mA.

8.5 Unused Pins

In case the VCC3 is not used in the application, it is recommended to connect the unused pins of VCC3 as followed:

- Connect VCC3SH to VS or leave open;
- Leave VCC3B open;
- Leave VCC3REF open
- Do not enable the VCC3 via SPI as this leads to increased current consumption

8.6 Electrical Characteristics

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; SBC Normal Mode; all outputs open; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Table 21 Electrical Characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			
Parameters independent from Test Set-up							
External Regulator Control Drive Current Capability	$I_{VCC3base}$	40	60	80	mA	$V_{VCC3base}$ = 13.5 V	
Input Current V_{CC3ref}	$I_{VCC3ref}$	0	3	10	µA	$V_{VCC3ref}$ = 5 V	
Input Current V_{CC3} Shunt Pin	$I_{VCC3shunt}$	–	–	10	µA	$V_{VCC3shunt}$ = V_S	

Output Current Shunt Voltage Threshold	$V_{shunt\_threshold}$	180	245	310	mV	1)	
Current increase regulation reaction time	t_{rlinc}	–	–	5	µs	5)V_{CC3} = 5V to 0V; $I_{CC3base}$ = 20 mA **Figure 26**	
Current decrease regulation reaction time	t_{rldec}	–	–	5	µs	5)V_{CC3} = 0 V to 5V; $I_{CC3base}$ = 20 mA **Figure 26**	
Leakage current of VCC3base when VCC3 disabled	$I_{VCC3base\_lk}$	–	–	5	µA	$V_{CC3base}$ = V_S; T_j = 25°C	
Leakage current of $V_{CC3shunt}$ when VCC3 disabled	$I_{VCC3shunt\_lk}$	–	–	5	µA	$V_{CC3shunt}$ = V_S; T_j = 25°C	
Base to emitter resistor	R_{BE}	120	150	185	kΩ	V_{CC3} = OFF;	
Active Peak Threshold VCC3 (Transition threshold between low-power and high-power mode regulator)	$I_{VCC3base,Ipeak,r}$	–	50	65	µA	5)Drive current $I_{VCC3base}$; $I_{VCC3base}$ rising V_S =13.5V; -40°C < T_j < 150°C	
Active Peak Threshold VCC3 (Transition threshold between high-power and low-power mode regulator)	$I_{VCC3base,Ipeak,f}$	15	30	–	µA	5)Drive current $I_{VCC3base}$; $I_{VCC3base}$ falling V_S =13.5V; -40°C < T_j < 150°C	
Parameters dependent on the Test Set-up (with external PNP device MJD-253)							
External Regulator Output Voltage	$V_{CC3.out1}$(5V)	4.9	5	5.1	V	2)SBC Normal Mode; load sharing configuration with 470 mΩ shunt resistor; 10 µA < I_{VCC1} + I_{VCC3} < 300 mA;	
	$V_{CC3.out1}$(3V3)	3.23	3.3	3.37			

Table 21 Electrical Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			
External Regulator Output Voltage (VCC3 = 5.0V)	$V_{CC3,out2}$	4.9	5	5.1	V	2)SBC Normal Mode; stand-alone configuration 10 mA < I_{VCC3} < 300 mA;	
External Regulator Output Voltage (VCC3 = 5.0V)	$V_{CC3,out3}$	4.8	5	5.2[4]	V	2)SBC Stop-, Sleep Mode; Stand-alone configuration 10µA < I_{VCC3} < $I_{VCC3\_peak,r}$[3]	
External Regulator Output Voltage (VCC3 = 3.3V)	$V_{CC3,out4}$	3.23	3.3V	3.37	V	2)SBC Normal Mode; stand-alone configuration 10 mA < I_{VCC3} < 300 mA;	
External Regulator Output Voltage (VCC3 = 3.3V)	$V_{CC3,out5}$	3.15	3.3V	3.45[4]	V	2)SBC Stop-, Sleep Mode; Stand-alone configuration 10µA < I_{VCC3} < $I_{VCC3\_peak,r}$[3]	

External Regulator Output Voltage (VCC3 = 1.8V)	$V_{CC3,out6}$	1.75	1.8V	1.85	V	2)SBC Normal Mode; stand-alone configuration 10 mA < I_{VCC3} < 300 mA;	
External Regulator Output Voltage (VCC3 = 1.8V)	$V_{CC3,out7}$	1.7	1.8	1.9 4)	V	2)SBC Stop-, Sleep Mode; Stand-alone configuration 10µA < I_{VCC3} < $I_{VCC3\_peak,r}$ 3)	
Load Sharing Ratio ICC1 : ICC3	$Ratio_{LS\_1,VCC3}$	1 : 1.35	1 : 1.9	1 : 2.45	–	5)6)6.0V < V_S < 28V; SBC Normal Mode; LS ratio for a 470 mΩ shunt resistor and total load current of 300mA	
Load Sharing Ratio ICC1 : ICC3	$Ratio_{LS\_2,VCC3}$	1 : 0.67	1 : 0.95	1 : 1.23	–	5)6)6.0V < V_S < 28V; SBC Normal Mode; LS ratio for a 1 Ω shunt resistor and total load current of 300mA	
Load Sharing Ratio ICC1 : ICC3	$Ratio_{LS\_3,VCC3}$	1 : 1.50	1 : 1.95	1 : 2.40	–	5)6) T_j = 150°C; 8.0V < V_S < 18V; SBC Normal Mode; LS ratio for a 470 mΩ shunt resistor and total load current of 300mA	
Load Sharing Ratio ICC1 : ICC3	$Ratio_{LS\_4,VCC3}$	1 : 0.75	1 : 0.98	1 : 1.21	–	5)6) T_j = 150°C; 8.0V < V_S < 18V; SBC Normal Mode; LS ratio for a 1 Ω shunt resistor and total load current of 300mA	

1) Threshold at which the current limitation starts to operate. This threshold is only active when VCC3 is configured for stand-alone configuration.
2) Tolerance includes load regulation and line regulation.
3) I_{VCC3_peak} refers to the load current out of the collector of the external PNP device. This value can be calculated by multiplying the VCC3base active peak threshold ($I_{VCC3base,Ipeak}$) with the current gain of the PNP
4) At T_j > 125°C, the power transistor leakage could be increased, which has to be added to the quiescent current of the application independently if the regulator is turned on/off. To prevent an overvoltage condition at no load due to this increased leakage, an internal clamping structure will automatically turn on at typ. 200mV above the upper limit of the programmed output voltage.
5) Not subject to production test, specified by design.
6) a) Ratio will change depending on the chosen shunt resistor which value is correlating to the maximum power dissipation of the PNP pass device. See **Chapter 8.4** for the ratio calculation. The ratio will also change at low-drop operation.
For supply voltages of 5.5V < VS < 6V the accuracy applies only for a total load current of 250mA.
The load sharing ratio in SBC Stop Mode has +/-10% wider limits than specified.

b) The output voltage precision in load sharing in SBC Stop Mode is according to VCC1 +/-4% or better for loads up to 20mA and +/-2% with loads greater than 20mA.
In SBC Normal the +/-2% precision for 5V/3.3V tolerance is valid regardless of the applied load.

Notes

1. There is no thermal protection available for the external PNP transistor. Therefore, the application must be designed to avoid overheating ofthe PNP via the shunt current limitation in standalone configuration and by selecting the proper ICC1/ICC3 ratio in load-sharing configuration.

2. In SBC Stop Mode, the same output voltage tolerance applies as in SBC Normal Mode when I_{VCC3} has exceeded the selected active peak threshold ($I_{VCC3base,Ipeak}$) but with increased current consumption.

Timing diagram for regulator reaction time “current increase regulation reaction time” and “current decrease regulation reaction time”

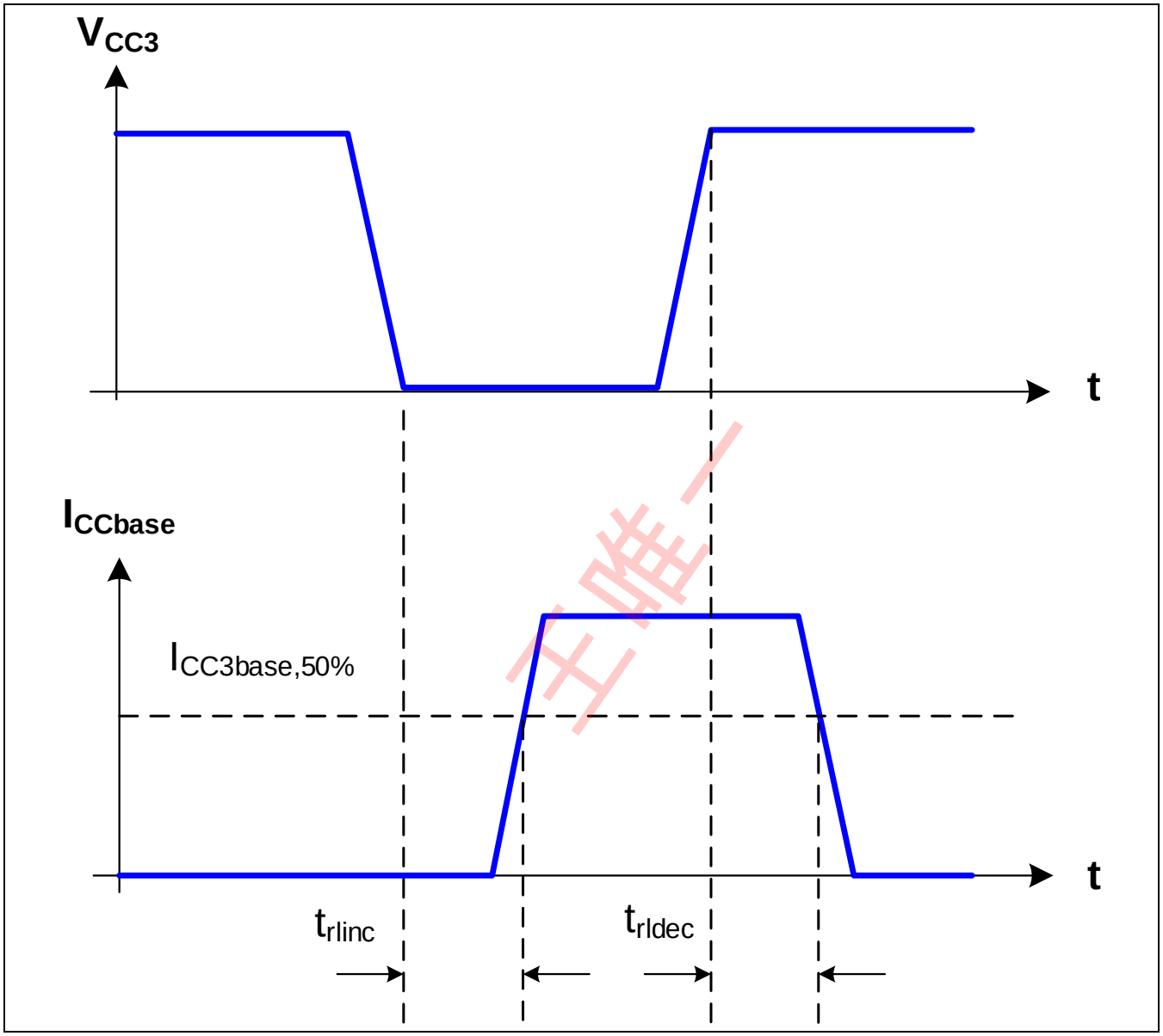


Figure 26 Regulator Reaction Time

Typical Load Sharing Characteristics using the BCP52-16 PNP transistor and a 1 Ω shunt resistor

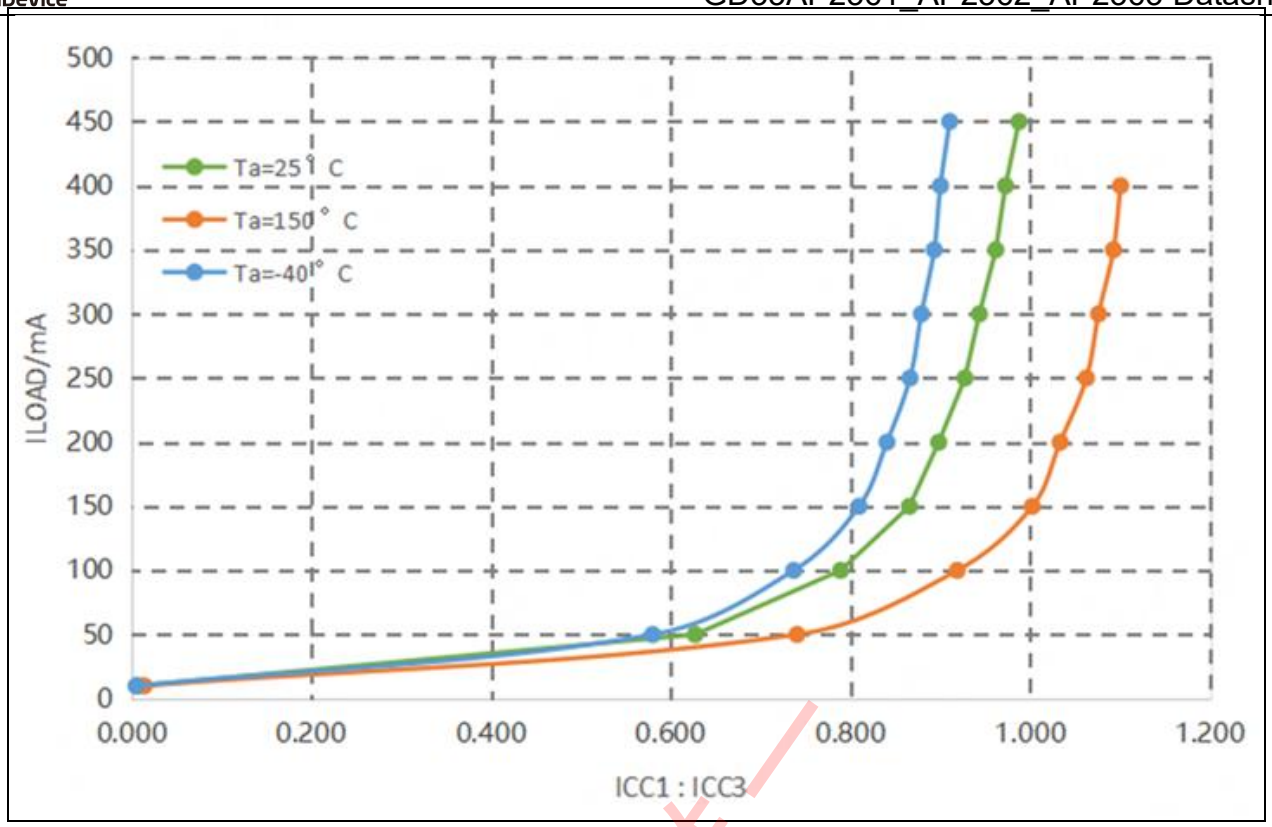


Figure 27 Typical Load Sharing Ratio ICC1 : ICC3 vs. the total load current

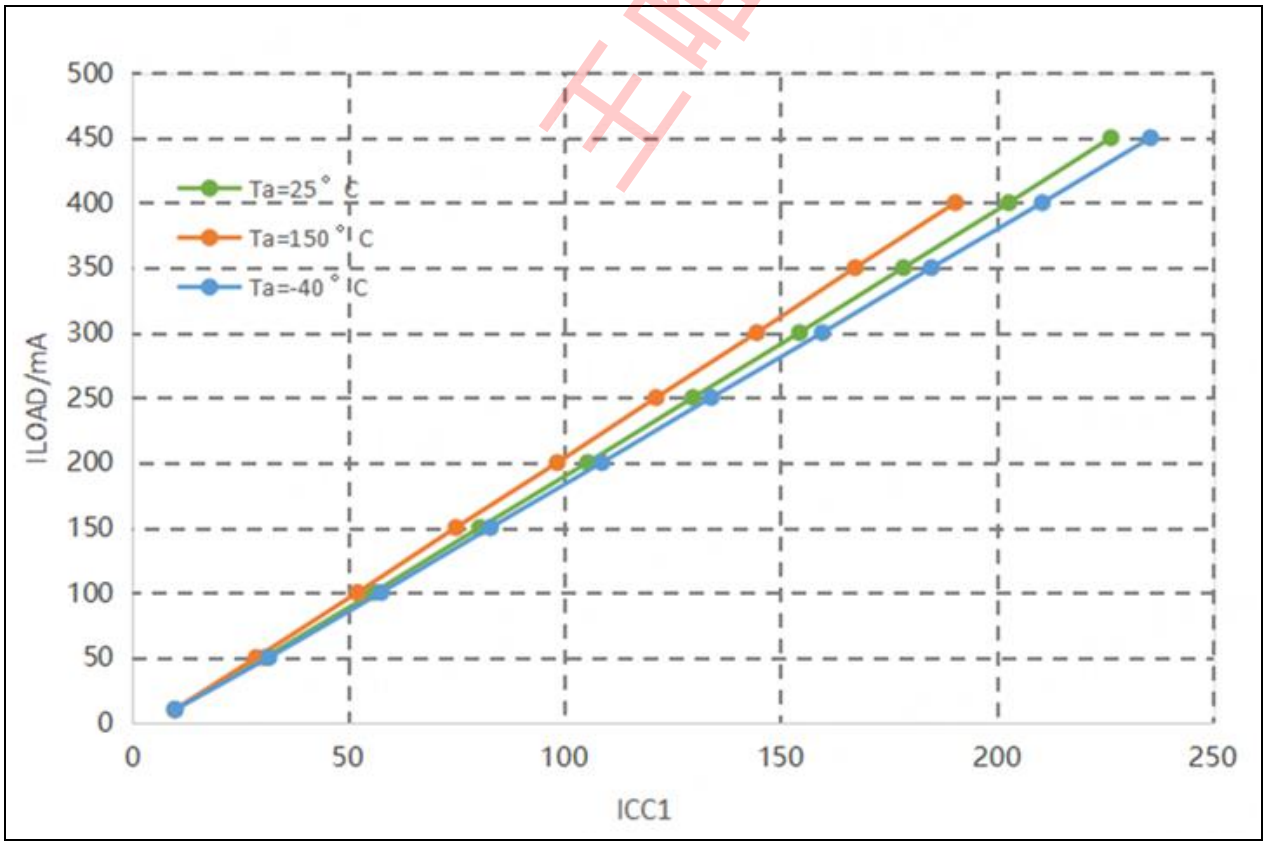


Figure 28 Typical Load Sharing Behavior of ICC1 vs. the total load current

9 High-Side Switch

9.1 Block Description

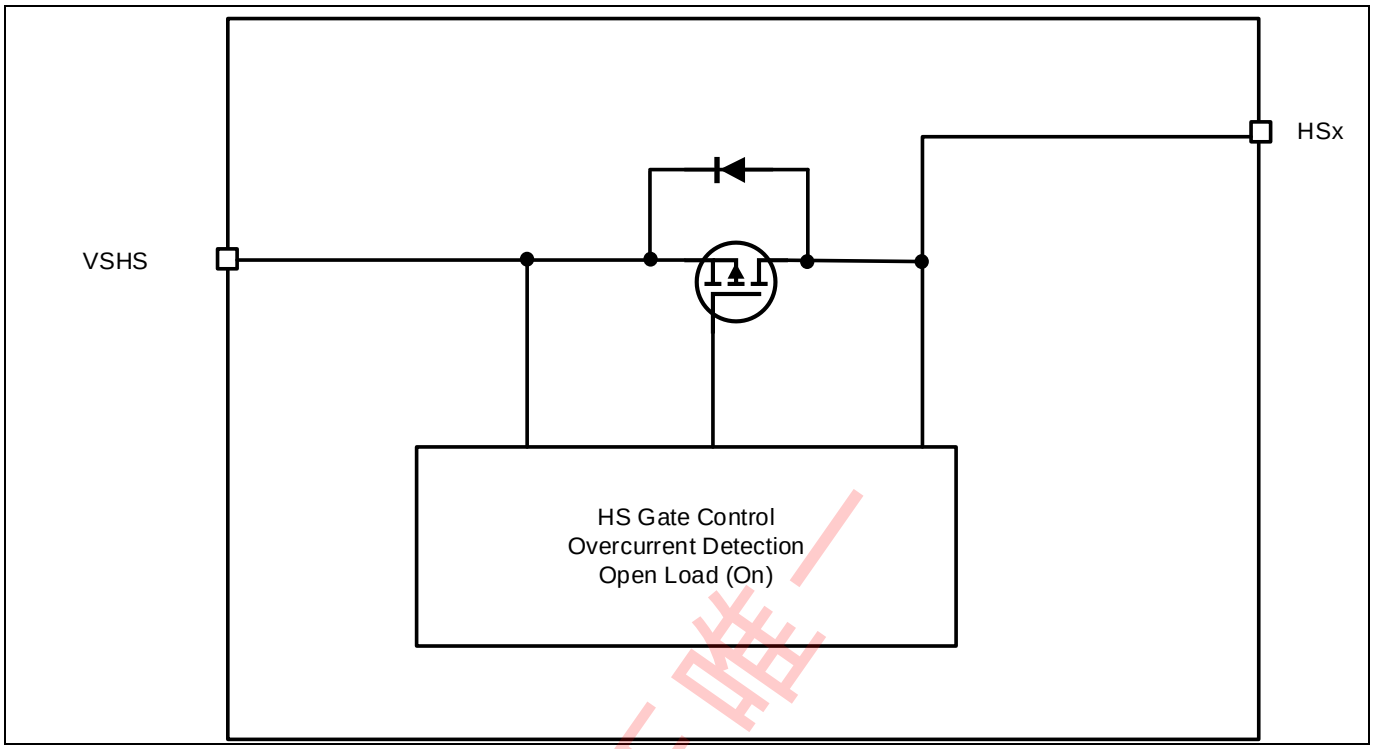


Figure 29 High-Side Module Block Diagram

Features

- Dedicated supply pin VSHS for high-side outputs
- Overvoltage and undervoltage switch off- configurable via SPI
- Overcurrent detection and switch off
- Open load detection in ON-state
- PWM capability with internal timer configurable via SPI
- Switch recovery after removal of OV or UV condition configurable via SPI

9.2 Functional Description

The High-Side switches can be utilized for driving LEDs, supplying wake inputs, or powering other loads. These outputs can be controlled either directly via SPI using the **HS_CTRL1** and **HS_CTRL2** registers, or by the integrated timers and PWM generators.

The High-Side outputs are powered from a dedicated supply pin VSHS, which is independent from VS, providing improved performance under cranking conditions.

The configuration of the High-Side drivers (e.g., Permanent On, PWM, Cyclic Sense, etc.) must be performed in SBC Normal Mode. Once configured, the settings are retained in SBC Stop or SBC Sleep Mode and cannot be modified. When the device enters SBC Restart Mode or SBC Fail-Safe Mode, all HSx outputs are automatically disabled.

9.2.1 Over-and Undervoltage Switch Off

All High-Side (HS) drivers that are in the *on-state* are switched off when an overvoltage condition occurs on VSHS (**V SHS,OVD**). Once the voltage falls below the overvoltage threshold, the HS drivers are automatically re-enabled. This protection feature can be disabled by setting the SPI bit **HS_OV_SD_EN**.

Similarly, the HS drivers are switched off when an undervoltage condition is detected on VSHS(**VSHS,UVD)**. When the voltage rises above the undervoltage threshold, the HS drivers are re-activated. This function can be disabled by setting the SPI bit **HS_UV_SD_EN**.

After the release of an overvoltage or undervoltage condition, the HS switches return to their previously programmed state as configured via SPI, provided that the bit **HS_OV_UV_REC** is set to '1'. If this bit is cleared ('0'), the HS switches remain off and the corresponding SPI control bits are reset.

The occurrence of overvoltage or undervoltage conditions is indicated by the status bits **VSHS_OV** and **VSHS_UV** respectively. No additional error bits are set.

9.2.2 Overcurrent Detection and Switch Off

If the load current exceeds the overcurrent shutdown threshold for a duration longer than the defined overcurrent filter time, the corresponding output is switched off.

The overcurrent condition and the resulting shutdown are indicated by the respective HSx_OC_OT bit in the **HS_OC_OT_STAT** register. Following this event, the HSx configuration is automatically reset to 000 by the SBC.

To reactivate the High-Side driver, the HSx configuration must be set to ON (001) or programmed for a timer-controlled operation. It is recommended to clear the overcurrent status bit before re-enabling the High-Side switch, as these bits are not cleared automatically by the SBC.

9.2.3 Open Load Detection

Open-load detection for the High-Side outputs is performed when the output is in the on-state. If the current through the active output drops below the defined Open-Load Detection threshold, an open-load condition is detected and indicated by the corresponding status bit (HS1_OL, HS2_OL, HS3_OL, or HS4_OL) in the **HS_OL_STAT** register.

During this condition, the High-Side output remains active. Once the open-load condition is no longer present, the respective Open-Load status bit can be cleared via SPI. These bits are not cleared automatically by the SBC.

9.2.4 HSx Operation in Different SBC Modes

- During SBC Stop Mode and SBC Sleep Mode, the HSx outputs can be utilized for the cyclic sense feature. The open-load detection, overcurrent shutdown, as well as overvoltage and undervoltage shutdown functions remain available in these modes. Note that the overcurrent shutdown protection may affect the wake-up behavior[1)].
- The HSx outputs can also be enabled during SBC Stop and SBC Sleep Mode, and can be controlled by the PWMx generator. Before entering any low-power mode, the HSx outputs must be configured in SBC Normal Mode.
- During SBC Restart Mode or SBC Fail-Safe Mode, the HSx outputs are switched off. They can be re-enabled via SPI once the failure condition has been cleared.

9.2.5 PWM and Timer Function

Two 8-bit PWM generators are dedicated to generate a PWM signal on the HS outputs, e.g. for brightness adjustment or compensation of supply voltage fluctuation. The PWM generators are mapped to the dedicated HS outputs, and the duty cycle can be independently configured with a 8bit resolution via SPI (**PWM1_CTRL**, **PWM2_CTRL**). Two different frequencies (200Hz, 400Hz) can be selected independently for every PWM generator in the register **PWM_FREQ_CTRL**.

1) For the wake feature, the forced overcurrent shutdown case must be considered in the user software for all SBC Modes, i.e. due to disabled HSx switches a level change might not be detected anymore at WKx pins.

PWM Assignment and Configuration:

- Configure duty cycle and frequency for respective PWM generator in **PWM1_CTRL**/**PWM2_CTRL** and **PWM_FREQ_CTRL**
- Assign PWM generator to respective HS switch(es) in HSx_CTRL

- The PWM generation will start right after the HSx is assigned to the PWM generator (**HS_CTRL1**, **HS_CTRL2**)

Assignment options of HS1... HS4

- Timer 1
- Timer 2
- PWM 1
- PWM 2

Minimum On-time during PWM Operation

The min. on-time during PWM is limited by the actual on- and off-time of the respective HS switch, e.g. the PWM setting '0000 0001' could not be realized.

Reliable Open-Load Detection during PWM Operation

The minimum PWM setting for a reliable open-load detection is 3digits for a period of 400Hz and >2 digits for the frequency setting of 200Hz,i.e. the high-side on-time must be longer than $t_{OL,HS}$.

Reliable Overcurrent Detection during PWM Operation

The minimum PWM setting for a reliable overcurrent detection is >1 digit for a period of 400Hz and 1 digit for the frequency setting of 200Hz,i.e. the high-side on-time must be longer than $t_{SD,HS}$.

9.3 Electrical Characteristics

Table 22 Electrical Characteristics

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			
Output HS1, HS2, HS3, HS4							
Static Drain-Source ON Resistance HS1...HS4	$R_{ON,HS25}$	–	7	10	Ω	I_{ds} = 60mA, T_j < 25°C	
Static Drain-Source ON Resistance HS1...HS4	$R_{ON,HS150}$	–	11.5	16	Ω	I_{ds} = 60mA, T_j < 150。 C	
Leakage Current HSx / per channel	$I_{leak,HS}$	–	–	2	µA	1)0 V < V_{HSx} < V_{SHS}; T_j < 85°C	
Output Slew Rate (rising)	$SR_{raise,HS}$	0.8	–	2.5	V/µs	1)20 to 80% V_{SHS} = 6 to 18V R_L = 220Ω	
Output Slew Rate (falling)	$SR_{fall,HS}$	-2.5	–	-0.8	V/µs	1)80 to 20% V_{SHS} = 6 to 18V R_L = 220Ω	
Switch-on time HSx	$t_{ON,HS}$	3	–	30	µs	CSN = HIGH to 0.8*VSHS; R_L = 220Ω; V_{SHS} = 6 to 18V	
Switch-off time HSx	$t_{OFF,HS}$	3	–	30	µs	CSN = HIGH to 0.2*VSHS; R_L = 220Ω; V_{SHS} = 6 to 18V	

Short Circuit Shutdown Current	$I_{SD,HS}$	150	245	300	mA	V_{SHS} = 6 to 20V, hysteresis included	
Short Circuit Shutdown Filter Time	$t_{SD,HS}$	12	16	20	µs	2), 3)	
Open Load Detection Current	$I_{OL,HS}$	0.4	–	3	mA	hysteresis included	
Open Load Detection hysteresis	$I_{OL,HS,hys}$	0.05	0.45	1.0	mA	1)	
Open Load Detection Filter Time	$t_{OL,HS}$	50	64	80	µs	2), 3)	

1) Not subject to production test, specified by design.

2) Not subject to production test, tolerance defined by internal oscillator tolerance.

3) Configure proper minimum PWM settings for reliable detection of overcurrent and open load measurement (see also **Chapter 9.2.5**).

10 High Speed CAN Transceiver

10.1 Block Description

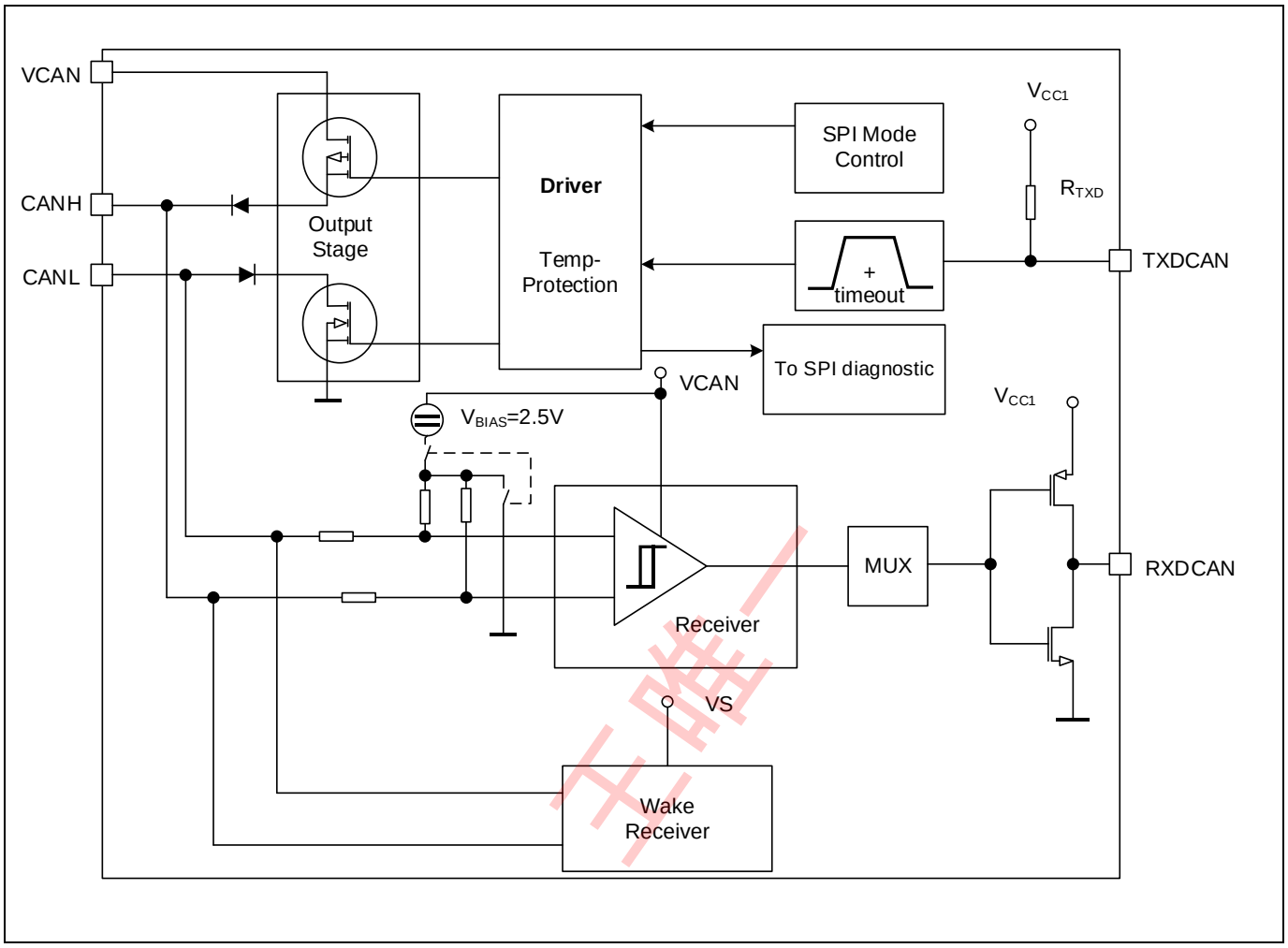


Figure 30 Functional Block Diagram

10.2 Functional Description

The CAN transceiver integrated in the System Basis Chip (SBC) enables high-speed (HS) differential data transmission and reception up to 2 Mbaud, suitable for automotive and industrial applications. It serves as the interface between the CAN protocol controller and the physical bus lines, fully compliant with ISO 11898-2:2016 and SAE J2284 standards.

To minimize current consumption, the transceiver provides several low-power operating modes, allowing operation in networks with partially powered-down nodes. A dedicated Receive-Only Mode is implemented to support software diagnostic functions.

When the transceiver is switched off, it exhibits excellent passive behavior, ensuring compatibility with mixed networks and clamp 15/30 applications.

A wake-up from the CAN wake-capable mode can be triggered by bus activity, enabling the microcontroller to remain in a low-power or idle state and be re-activated by CAN communication.

Designed to withstand the harsh conditions of automotive environments, the CAN transceiver fully supports 12 V system applications.

The different transceiver modes can be controlled via the SPI **CAN** bits.

Figure 31 shows the possible transceiver mode transitions when changing the SBC mode.

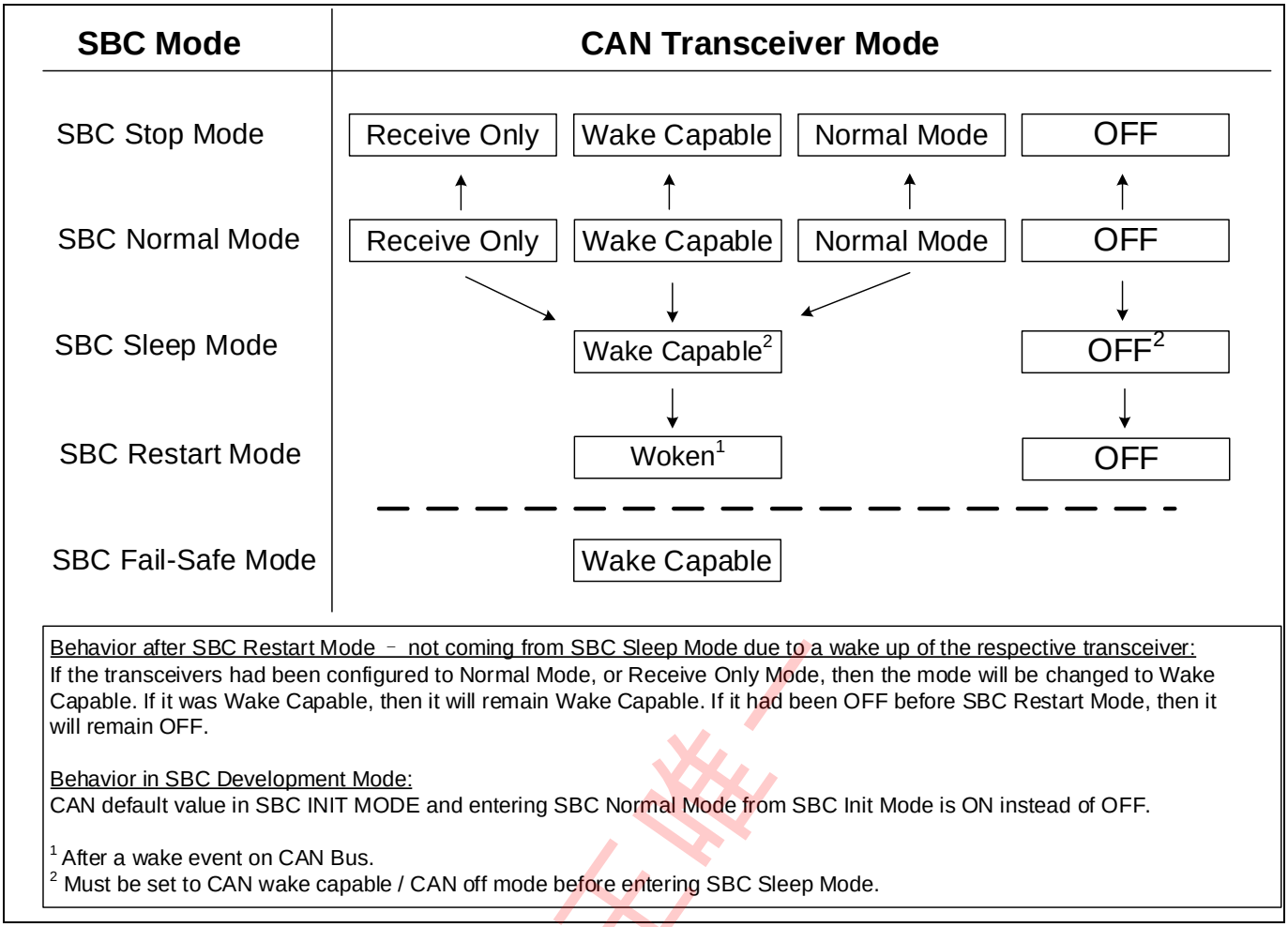


Figure 31 CAN Mode Control Diagram

CAN FD Support

CAN FD stands for 'CAN with Flexible Data Rate'. It is based on the well established CAN protocol as specified in ISO 11898-1. CAN FD still uses the CAN bus arbitration method. The benefit is that the bit rate can be increased by switching to a shorter bit time at the end of the arbitration process and then to return to the longer bit time at the CRC delimiter, before the receivers transmit their acknowledge bits. See also **Figure 32**. In addition, the effective data rate is increased by allowing longer data fields. CAN FD allows the transmission of up to 64 data bytes compared to the 8 data bytes from the standard CAN.

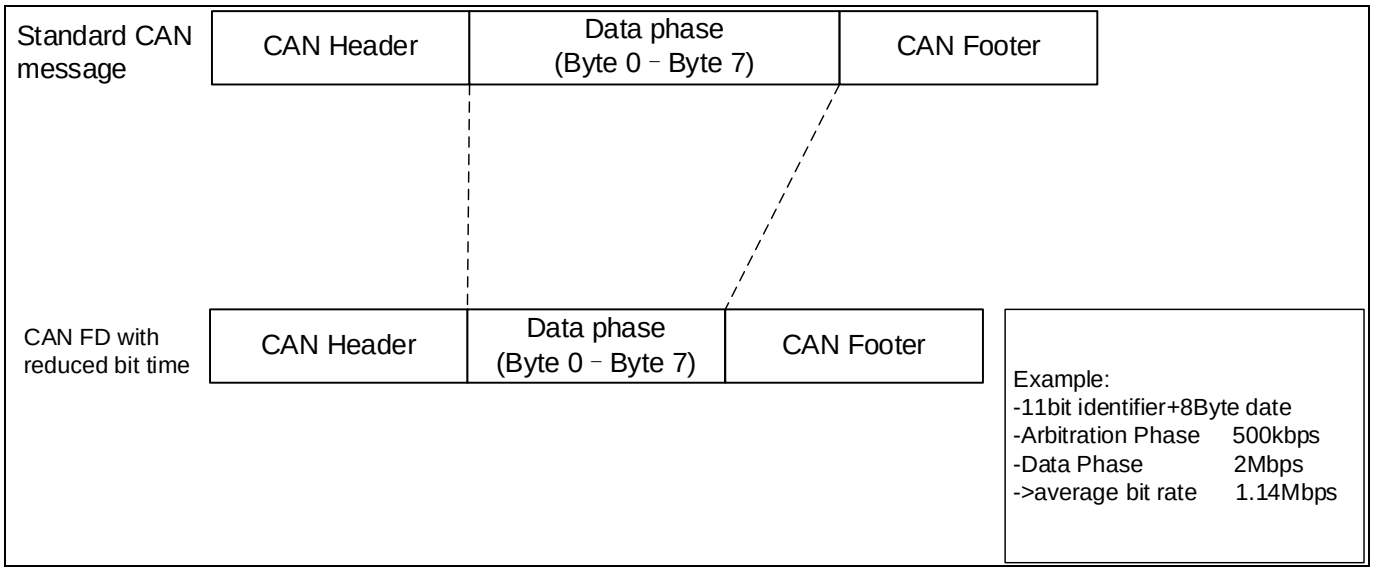


Figure 32 Bite Rate Increase with CAN FD vs. Standard CAN

Both the physical layer and the CAN controller must support CAN FD communication. If the CAN controller does not support CAN FD operation, the corresponding CAN node must at least be tolerant to CAN FD communication.

The CAN FD tolerant mode is implemented at the physical layer in combination with CAN Partial Networking, ensuring compatibility within mixed CAN and CAN FD environments.

The GD33AP236x-3QV variants of this device family also support the CAN FD tolerant mode. For detailed information on enabling this mode, refer to **Chapter 5.4.7**.

10.2.1 CAN OFF Mode

The CAN OFF Mode is the default operating state after the power-up of the System Basis Chip (SBC). It is available in all SBC operating modes and is intended to completely disable all CAN activities when CAN communication is not required.

In this mode, the CANH/CANL bus interface behaves as a high-impedance input with minimal leakage current. Any wake-up events occurring on the bus are ignored while the device remains in CAN OFF Mode.

10.2.2 CAN Normal Mode

The CAN transceiver is activated via SPI when the SBC operates in Normal Mode. The CAN Normal Mode is designed for standard high-speed CAN (HS-CAN) data transmission and reception. This mode is available in both SBC Normal Mode and SBC Stop Mode, with the bus bias voltage set to VCAN / 2.

Transmission

The TXDCAN input signal from the microcontroller is applied to the SBC, and the bus driver converts this signal by switching the CANH and CANL output stages to transmit the corresponding logic levels onto the CAN bus.

Enabling sequence

Before a message can be transmitted, the CAN transceiver requires an enable time ($t_{CAN,EN}$). The TXDCAN signal must remain recessive (HIGH) until this enable period has elapsed. If this condition is not met, the TXDCAN line must first be returned to the recessive state before transmission can proceed. After the enabling time is completed.

Only the next dominant bit will be transmitted on the bus.

Figure 33 shows different scenarios and explanations for CAN enabling.

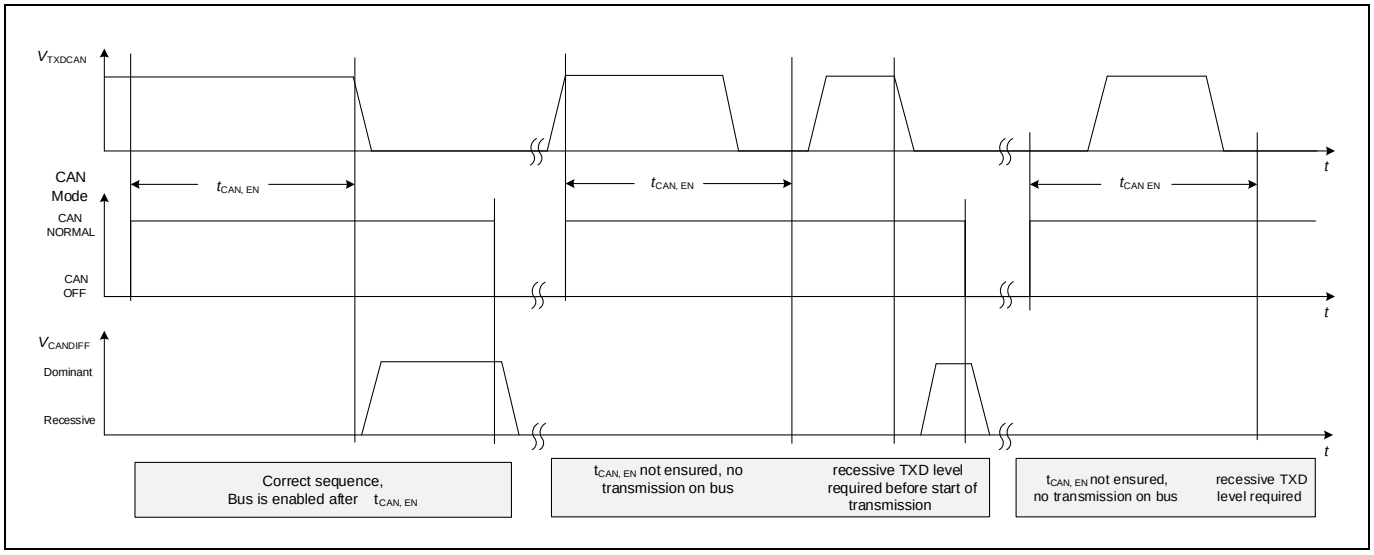


Figure 33 CAN Transceiver Enabling Sequence

Reduced Electromagnetic Emission

To reduce electromagnetic emissions (EME), the bus driver controls CANH/L slopes symmetrically.

Reception

Analog CAN bus signals are converted into digital signals at RXD via the differential input receiver.

10.2.3 CAN Receive Only Mode

In CAN Receive Only Mode (RXD only), the driver stage is de-activated but reception is still operational. This mode is accessible by an SPI command in Normal Mode and in Stop Mode. The bus biasing is set to VCAN/2.

In CAN Receive-Only Mode (RXD-only), the driver stage of the transceiver is disabled, while the reception path remains fully operational. This mode can be activated via an SPI command when the SBC is in either Normal Mode or Stop Mode. The bus biasing in this state is set to VCAN / 2.

10.2.4 CAN Wake Capable Mode

The CAN Wake-Capable Mode is used to monitor bus activity and can be enabled in SBC Stop, Sleep, Restart, and Normal Modes. It is also automatically entered when the SBC transitions to Fail-Safe Mode. In this mode, both CANH and CANL pins are connected to GND through input resistors.

When a wake-up signal is detected on the bus, the SBC's behavior changes accordingly, as specified in Table 23. The CANH/L pins are terminated to approximately 2.5 V through the input resistors. As an indication to the microcontroller, the RXD_CAN pin is pulled LOW and remains LOW until the CAN transceiver is switched to another mode. After a wake-up event, the transceiver can be set to CAN Normal Mode via SPI to resume standard CAN communication.

As illustrated in **Figure 34**, a wake-up pattern (WUP) is recognized on the bus when two consecutive dominant levels occur for a duration of at least t_{Wake1} (filter time $t > t_{Wake1}$) and shorter than t_{Wake2}, each separated by a recessive level lasting longer than t_{Wake1} but shorter than t_{Wake2}.

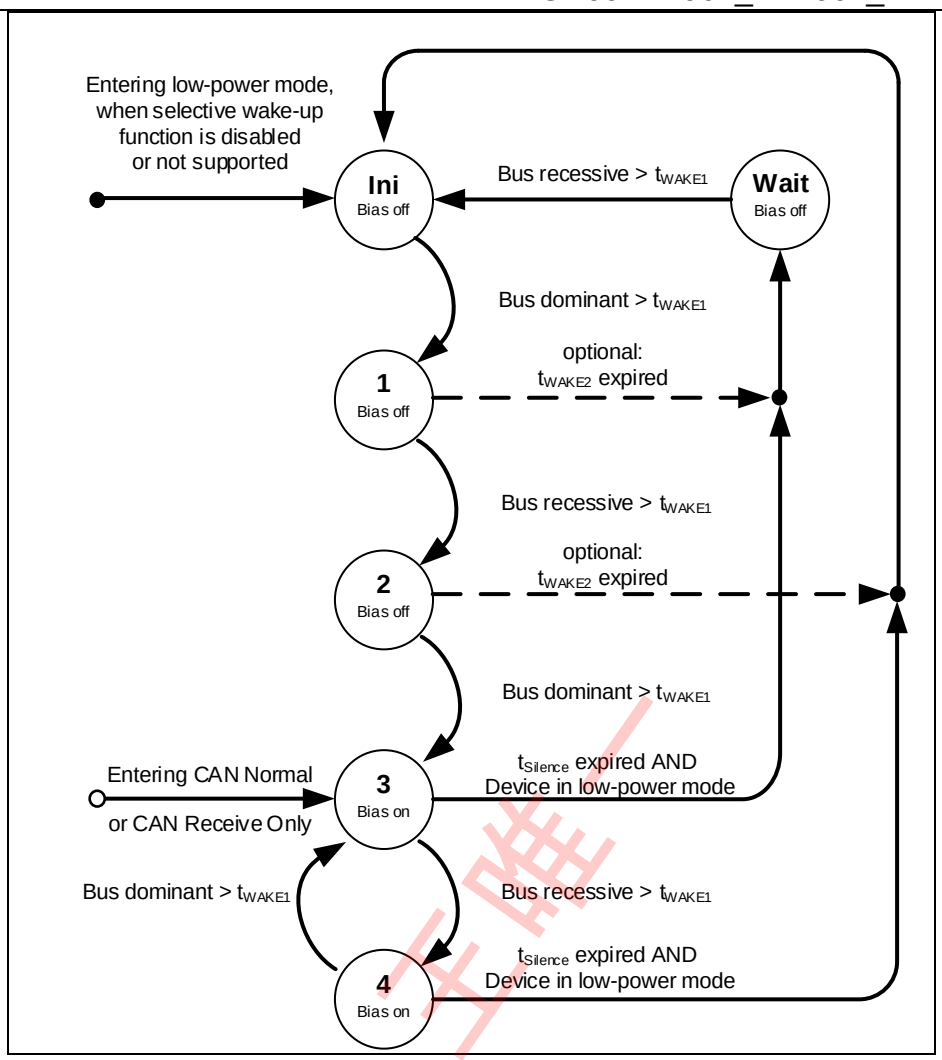


Figure 34 WUP detection following the definition in ISO 11898-2:2016

Rearming the Transceiver for Wake Capability

After a bus wake-up event, the CAN transceiver becomes active. However, the **CAN** transceiver mode bits will still indicate Wake-Capable Mode (= '01'), keeping the RXD signal in the LOW state. There are two ways to re-enable the CAN Wake-Capable Mode after a wake-up event:

- The CAN transceiver mode must be toggled, i.e., switched from Wake-Capable Mode to CAN Normal Mode, CAN Receive-Only Mode, or CAN OFF Mode, before being set back to CAN Wake-Capable Mode.
- Automatic re-arming occurs when the SBC transitions to SBC Stop Mode or SBC Fail-Safe Mode, ensuring continuous wake-up capability.
- Before entering SBC Sleep Mode, the CAN must be configured to either CAN Wake-Capable Mode or CAN OFF Mode.

Notes:

1. It is not required to clear the CAN wake-up flag (**CAN_WU**) to restore wake-capable functionality; simply toggling the CAN mode is sufficient.
2. In CAN Wake-Capable Mode, the CAN module is powered by an internal supply voltage, meaning it does not require VCAN during this state. Before switching the CAN mode back to Normal Mode, the VCAN supply must be enabled.

Wake-Up in SBC Stop and Normal Mode

In SBC Stop Mode, when a wake-up event is detected, it is indicated by both the INT output and the **WK_STAT_1** SPI register. Additionally, the RXDCAN pin is driven LOW to signal the wake-up condition. The same behavior applies when the device operates in SBC Normal Mode.

After a wake-up in SBC Stop Mode, the microcontroller must manually switch the SBC from Stop Mode to Normal Mode, as no automatic transition occurs.

For functional safety, if the watchdog was previously disabled, it will be automatically re-enabled in SBC Stop Mode following a bus wake-up event, provided that the **WD_EN_ WK_BUS** bit was configured to HIGH beforehand.

Wake-Up in SBC Sleep Mode

In SBC Sleep Mode, a wake-up can be triggered by a CAN message meeting the filter time condition ($t > t_{Wake1}$). Upon wake-up, the SBC automatically transitions first to SBC Restart Mode, and then to Normal Mode. During this process, the RXD pin is set LOW, enabling the microcontroller to detect the wake-up event.

The wake source can be identified by reading the **WK_STAT_1** register via SPI. No interrupt signal is generated when exiting Sleep Mode. Subsequently, the microcontroller can activate CAN Normal Mode through SPI to resume standard CAN communication.

Table 23 Action due to CAN Bus Wake-Up

SBC Mode	SBC Mode after Wake	VCC1	INT	RXD
Normal Mode	Normal Mode	ON	LOW	LOW
Stop Mode	Stop Mode	ON	LOW	LOW
Sleep Mode	Restart Mode	Ramping Up	HIGH	LOW
Restart Mode	Restart Mode	ON	HIGH	LOW
Fail-Safe Mode	Restart Mode	Ramping up	HIGH	LOW

10.2.5 TXD Time-out Feature

In CAN Normal Mode, if the TXD signal remains dominant for a duration $t > t_{TXD\_CAN\_TO}$, the TXD time-out function deactivates the transmission on the bus. This mechanism prevents the bus from being permanently blocked due to a transmission error.

When the time-out condition occurs, the transmitter stage is disabled, and the transceiver automatically switches to Receive-Only Mode. The failure condition is recorded in the SPI flag **CAN_FAIL**.

Once the dominant state is removed, the CAN transmitter is reactivated, and the transceiver automatically returns to CAN Normal Mode. The overall transceiver configuration remains unchanged throughout this process.

10.2.6 Bus Dominant Clamping

If the HS-CAN bus remains dominant for a period $t > t_{BUS\_CAN\_TO}$ while operating in CAN Normal Mode or Receive-Only Mode, a bus dominant clamping condition is detected. In this case, the SPI bit **CAN_FAIL** is set, indicating the fault.

The transceiver configuration remains unchanged under this condition.

10.2.7 Undervoltage Detection

The VCAN supply voltage is continuously monitored when the transceiver operates in CAN Normal Mode or Receive-Only Mode, during SBC Normal and Stop Modes. If an undervoltage condition is detected ($VCAN < V_{CAN\_UV}$), the SPI bit VCAN_UV is set, and the SBC disables the transmitter stage.

When the CAN supply voltage rises above the undervoltage threshold ($VCAN > V_{CAN\_UV}$), the transceiver is automatically switched back to CAN Normal Mode. The transceiver configuration remains unchanged during this recovery process.

10.3 Electrical Characteristics

Table 24 Electrical Characteristics

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; 4.75 V < V_{CAN} < 5.25 V; R_L = 60Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			
CAN Bus Receiver							
Differential Receiver Threshold Voltage, recessive to dominant edge	V_{diff,rd_N}	–	0.80	0.90	V	$V_{diff} = V_{CANH} - V_{CANL}$; -12V ≤ V_{CM}(CAN) ≤ +12V; 0.9 V ≤ V_{diff,D_Range} ≤ 8 V; CAN Normal Mode	
Dominant state differential input voltage range	$V_{diff\_D\_range}$	0.9	–	8.0	V	1) $V_{diff} = V_{CANH} - V_{CANL}$; -12V ≤ V_{CM}(CAN) ≤ +12V; CAN Normal Mode	
Differential Receiver Threshold Voltage, dominant to recessive edge	V_{diff,dr_N}	0.50	0.60	–	V	$V_{diff} = V_{CANH} - V_{CANL}$; -12V ≤ V_{CM}(CAN) ≤ +12V; -3 V ≤ V_{diff,R_Range} ≤ 0.5 V; CAN Normal Mode	
Recessive state differential input voltage range	$V_{diff\_R\_range}$	-3.0	–	0.5	V	1) $V_{diff} = V_{CANH} - V_{CANL}$; -12V ≤ V_{CM}(CAN) ≤ +12V; CAN Normal Mode	
Common Mode Range	CMR	-12	–	12	V	1)	
CANH, CANL Input Resistance	R_{in}	20	40	50	kΩ	CAN Normal / Wake capable Mode; Recessive state; -2 V ≤ $V_{CANL/H}$ ≤ +7 V	
Differential Input Resistance	R_{diff}	40	80	100	kΩ	CAN Normal / Wake capable Mode; Recessive state; -2 V ≤ $V_{CANL/H}$ ≤ +7 V	
Input Resistance Deviation between CANH and CANL	ΔR_i	-3	–	3	%	1) Recessive state; $V_{CANH} = V_{CANL}$ = 5 V	
Input Capacitance CANH, CANL versus GND	C_{in}	–	20	40	pF	2) V_{TXD} = 5 V	
Differential Input Capacitance	C_{diff}	–	10	20	pF	2) V_{TXD} = 5 V	
Wake-up Receiver Threshold Voltage, recessive to dominant edge	$V_{diff,\ rd\_W}$	–	0.8	1.15	V	-12V ≤ V_{CM}(CAN) ≤ +12V; 1.15 V ≤ V_{diff,D_Range} ≤ 8 V; CAN Wake Capable Mode	

Table 24 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; 4.75 V < V_{CAN} < 5.25 V; R_L = 60Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			

Wake-up Receiver Dominant state differential input voltage range	V_{diff,D_range_W}	1.15	–	8.0	V	1)-12V ≤ V_{CM}(CAN) ≤ +12V; CAN Wake Capable Mode	
Wake-up Receiver Threshold Voltage, dominant to recessive edge	$V_{diff,\ dr\_W}$	0.4	0.7	–	V	-12V ≤ V_{CM}(CAN) ≤ +12V; -3 V ≤ V_{diff,R_Range} ≤ 0.4 V; CAN Wake Capable Mode	
Wake-up Receiver Recessive state differential input voltage range	V_{diff,R_range_W}	-3.0	–	0.4	V	1)-12V ≤ V_{CM}(CAN) ≤ +12V; CAN Wake Capable Mode	
CAN Bus Transmitter							
CANH/CANL Recessive Output Voltage (CAN Normal Mode)	V_{CANL/H_NM}	2.0	–	3.0	V	CAN Normal Mode; V_{TXD} = V_{CC1}; no load	
CANH/CANL Recessive Output Voltage (CAN Wake Capable Mode)	V_{CANL/H_LP}	-0.1	–	0.1	V	CAN Wake Capable Mode; V_{TXD} = V_{CC1}; no load	
CANH, CANL Recessive Output Voltage Difference V_{diff} = V_{CANH} - V_{CANL} (CAN Normal Mode)	$V_{diff\_r\_N}$	-500	–	50	mV	CAN Normal Mode V_{TXD} = V_{CC1}; no load	
CANH, CANL Recessive Output Voltage Difference V_{diff} = V_{CANH} - V_{CANL} (CAN Wake Capable Mode)	$V_{diff\_r\_W}$	-200	–	200	mV	CAN Wake Capable Mode; V_{TXD} = V_{CC1}; no load	
CANL Dominant Output Voltage	V_{CANL}	0.5	–	2.25	V	CAN Normal Mode; V_{TXD} = 0 V; V_{CAN} = 5 V; 50Ω ≤ R_L ≤ 65Ω	
CANH Dominant Output Voltage	V_{CANH}	2.75	–	4.5	V	CAN Normal Mode; V_{TXD} = 0 V; V_{CAN} = 5 V; 50Ω ≤ R_L ≤ 65Ω	
CANH, CANL Dominant Output Voltage Difference V_{diff} = V_{CANH} - V_{CANL}	$V_{diff\_d\_N}$	1.5	2.0	2.5	V	CAN Normal Mode; V_{TXD} = 0 V; V_{CAN} = 5 V; 50Ω ≤ R_L ≤ 65Ω	

Table 24 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; 4.75 V < V_{CAN} < 5.25 V; R_L = 60Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			

CANH, CANL Dominant Output Voltage Difference $V_{diff} = V_{CANH} - V_{CANL}$	$V_{diff\_d\_N}$	1.5	–	5.0	V	1)CAN Normal Mode; V_{TXD} = 0 V; V_{CAN} = 5 V; R_L = 2240Ω	
CANH, CANL Dominant Output Voltage Difference $V_{diff} = V_{CANH} - V_{CANL}$	$V_{diff\_d\_N}$	1.4	–	3.3	V	1)CAN Normal Mode; V_{TXD} = 0 V; V_{CAN} = 5 V; 45Ω ≤ R_L ≤ 70Ω	
CANH, CANL output voltage difference slope, recessive to dominant	$V_{diff\_slope\_rd}$	–	–	70	V/us	1)30% to 70% of measured differential bus voltage, C_L = 100 pF, R_L = 60 Ω	
CANH, CANL output voltage difference slope, dominant to recessive	$V_{diff\_slope\_dr}$	–	–	70	V/us	1)70% to 30% of measured differential bus voltage, C_L = 100 pF, R_L = 60 Ω	
Driver Symmetry $V_{SYM} = V_{CANH} + V_{CANL}$	V_{SYM}	4.5	–	5.5	V	3)CAN Normal Mode; V_{TXD} = 0 V / 5 V; V_{CAN} = 5 V; C_{SPLIT} = 4.7nF; R_L = 60Ω;	
CANH Short Circuit Current	I_{CANHsc}	-115	-80	-50	mA	CAN Normal Mode; $V_{CANHshort}$ = -3 V	
CANL Short Circuit Current	I_{CANLsc}	50	80	115	mA	CAN Normal Mode $V_{CANLshort}$ = 18 V	
Leakage Current (unpowered device)	$I_{CANH,lk}$ $I_{CANL,lk}$	–	5	7.5	µA	$V_S = V_{CAN}$ = 0V; 0V < $V_{CANH,L}$ ≤ 5V; 4)R_{test} = 0 / 47 kΩ	
Receiver Output RXD							
HIGH level Output Voltage	$V_{RXD,H}$	0.8 × V_{CC1}	–	–	V	CAN Normal Mode $I_{RXD(CAN)}$ = -2 mA;	
LOW Level Output Voltage	$V_{RXD,L}$	–	–	0.2 × V_{CC1}	V	CAN Normal Mode $I_{RXD(CAN)}$ = 2 mA;	
Transmission Input TXD							
HIGH Level Input Voltage Threshold	$V_{TXD,H}$	–	–	0.7 × V_{CC1}	V	CAN Normal Mode recessive state	

Table 24 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; 4.75 V < V_{CAN} < 5.25 V; R_L = 60Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			
LOW Level Input Voltage Threshold	$V_{TXD,L}$	0.3 × V_{CC1}	–	–	V	CAN Normal Mode dominant state	

TXD Input Hysteresis	$V_{TXD,hys}$	0.08 × V_{CC1}	0.12 × V_{CC1}	0.5 × V_{CC1}	V	1)	
TXD Pull-up Resistance	R_{TXD}	20	40	80	kΩ	–	
CAN Transceiver Enabling Time	$t_{CAN,EN}$	8	13	18	µs	5)CSN = HIGH to first valid transmitted TXD dominant	
Dynamic CAN-Transceiver Characteristics							
Min. Dominant Time for Bus Wake-up	t_{Wake1}	0.50	–	1.8	µs	-12V ≤ V_{CM}(CAN) ≤ +12V; CAN Wake capable Mode	
Wake-up Time-out, Recessive Bus	t_{Wake2}	0.8	–	10	ms	5)CAN Wake capable Mode	
WUP Wake-up Reaction Time	t_{WU_WUP}	–	–	100	µs	5)6)7) Wake-up reaction time after a valid WUP on CAN bus;	
Loop delay (recessive to dominant)	$t_{LOOP,f}$	–	150	255	ns	3)CAN Normal Mode C_L = 100 pF; R_L = 60 Ω; V_{CAN} = 5 V; C_{RXD} = 15 pF	
Loop delay (dominant to recessive)	$t_{LOOP,r}$	–	150	255	ns	3)CAN Normal Mode C_L = 100 pF; R_L = 60 Ω; V_{CAN} = 5 V; C_{RXD} = 15 pF	
Propagation Delay TXD LOW to bus dominant	$t_{d(L),T}$	–	50	–	ns	CAN Normal Mode C_L = 100pF; 50Ω ≤ R_L ≤ 65Ω; V_{CAN} = 5 V;	
Propagation Delay TXD HIGH to bus recessive	$t_{d(H),T}$	–	50	–	ns	CAN Normal Mode C_L = 100 pF; 50Ω ≤ R_L ≤ 65Ω; V_{CAN} = 5 V;	
Propagation Delay bus dominant to RXD LOW	$t_{d(L),R}$	–	100	–	ns	CAN Normal Mode C_L = 100pF; 50Ω ≤ R_L ≤ 60Ω; V_{CAN} = 5 V; C_{RXD} = 15 pF	

Table 24 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; 4.75 V < V_{CAN} < 5.25 V; R_L = 60Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			

Propagation Delay bus recessive to RXD HIGH	$t_{d(H),R}$	–	100	–	ns	CAN Normal Mode C_L = 100pF; 50Ω ≤ R_L ≤ 60Ω; V_{CAN} = 5 V; C_{RXD} = 15 pF	
Received Recessive Bit Width (CAN FD up to 2Mbps)	$t_{bit(RXD)}$	400	–	550	ns	CAN Normal Mode C_L = 100pF; R_L = 60 Ω; V_{CAN} = 5 V; C_{RXD} = 15 pF; $t_{bit(TXD)}$ = 500ns; Timing definition according to **Figure 36**	
TransmittedRecessive Bit Width (CAN FD up to 2Mbps)	$t_{bit(BUS)}$	435	–	530	ns	CAN Normal Mode C_L = 100pF; R_L = 60 Ω; V_{CAN} = 5 V; C_{RXD} = 15 pF; $t_{bit(TXD)}$ = 500ns; Timing definition according to **Figure 36**	
Receiver Timing Symmetry (CAN FD up to 2Mbps)	Δt_{Rec}	-65	–	40	ns	CAN Normal Mode C_L = 100pF; R_L = 60 Ω; V_{CAN} = 5 V; C_{RXD} = 15 pF; $t_{bit(TXD)}$ = 500ns; Timing definition according to **Figure 36**	
Received Recessive Bit Width (CAN FD up to 5 Mbps)	$t_{bit(RXD)}$	120	–	220	ns	CAN Normal Mode; C_L = 100pF; R_L = 60 Ω; V_{CAN} = 5 V; C_{RXD} = 15 pF; $t_{bit(TXD)}$ = 200 ns; Parameter definition in according to **Figure 36**.	

Table 24 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; 4.75 V < V_{CAN} < 5.25 V; R_L = 60Ω; CAN Normal Mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	**Symbol**	**Values**			**Unit**	**Note or Test Condition**	**Note**
		Min.	**Typ.**	**Max.**			

Transmitted Recessive Bit Width (CAN FD up to 5 Mbps)	$t_{bit(BUS)}$	155	–	210	ns	CAN Normal Mode; C_L = 100pF; R_L = 60Ω; V_{CAN} = 5 V; C_{RXD} = 15 pF; $t_{bit(TXD)}$ = 200 ns; Parameter definition in according to **Figure 36**.	
Receiver Timing Symmetry (CAN FD up to 5 Mbps)	Δt_{Rec}	-45	–	15	ns	CAN Normal Mode; C_L = 100pF; R_L = 60Ω; V_{CAN} = 5 V; C_{RXD} = 15 pF; $t_{bit(TXD)}$ = 200 ns; Parameter definition in according to **Figure 36**.	
TXD Permanent Dominant Time-out	$t_{TxD\_CAN\_TO}$	1.6	2	2.4	ms	5)CAN Normal Mode	
BUS Permanent Dominant Time-out	$t_{BUS\_CAN\_TO}$	1.6	2	2.4	ms	5)CAN Normal Mode	
Timeout for bus inactivity	$t_{SILENCE}$	0.6	–	1.2	s	5)	
Bus Bias reaction time	t_{Bias}	–	–	200	µs	5)	

1) Not subject to production test, specified by design.
2) Not subject to production test, specified by design, S2P - Method; f= 10 MHz.
3) $\mathbf{V_{SYM}}$ shall be observed during dominant and recessive state and also during the transition dominant to recessive and vice versa while TXD issimulated by a square signal (50% duty cycle) with a frequency of up to 1 MHz (2 MBit/s).
4) R_{test} between supply (VS / VCAN) and 0V (GND).
5) Not subject to production test, tolerance defined by internal oscillator tolerance.
6) Wake-up is signalized via INT pin activation in SBC Stop Mode and via VCC1 ramping up with wake from SBC Sleep Mode.
7) Time starts with end of last dominant phase of WUP.

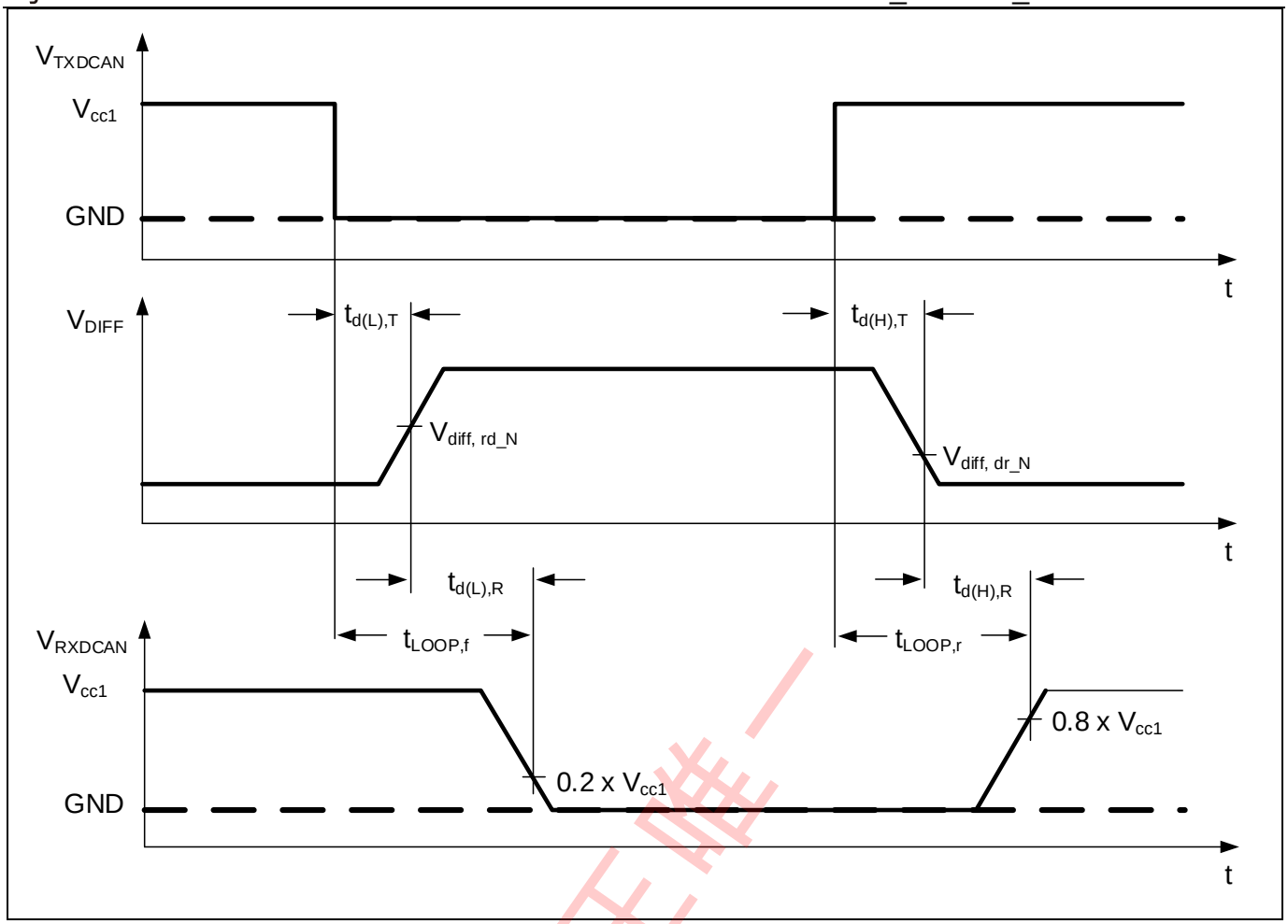


Figure 35 Timing Diagrams for Dynamic Characteristics

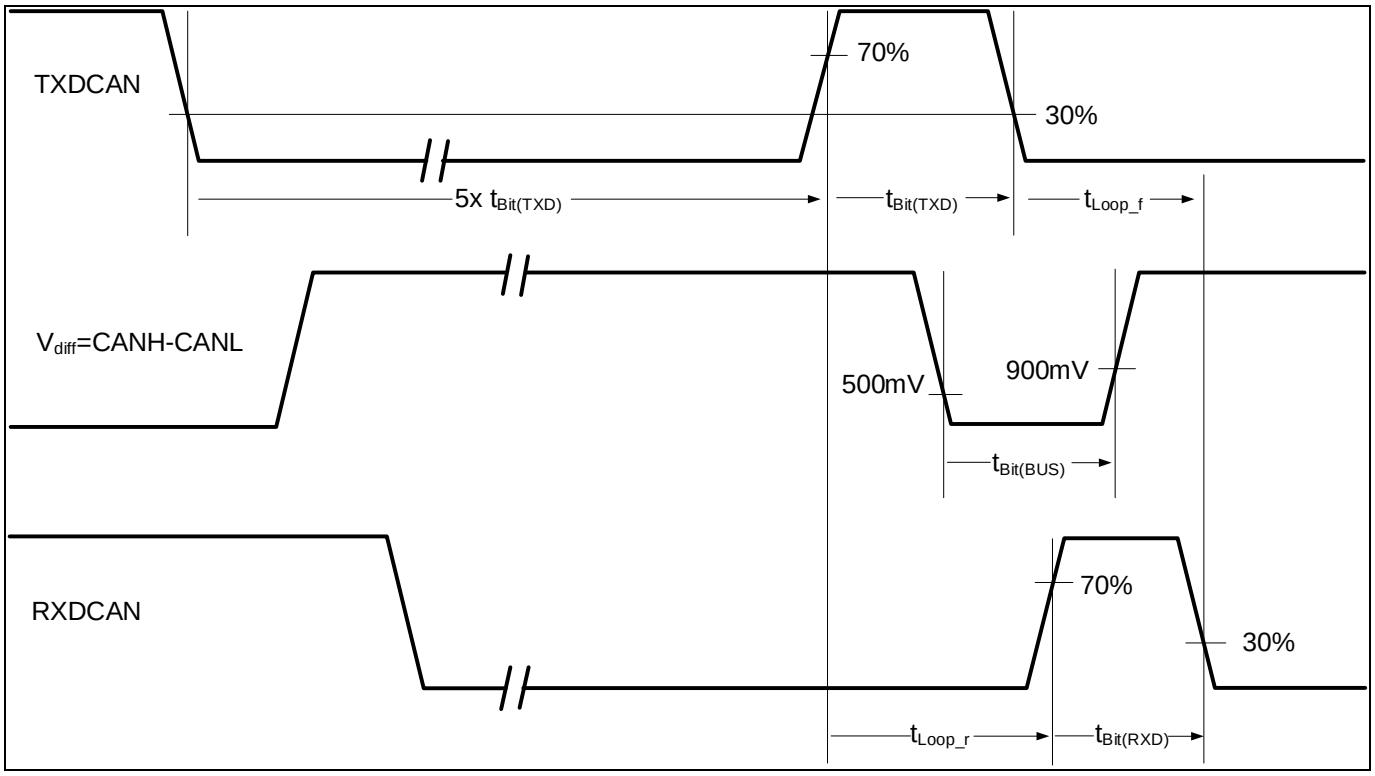


Figure 36 From ISO 11898-2: t_{loop}, $t_{bit(TXD)}$, $t_{bit(Bus)}$, $t_{bit(RXD)}$ definitions

11 LIN Transceiver

11.1 Block Description

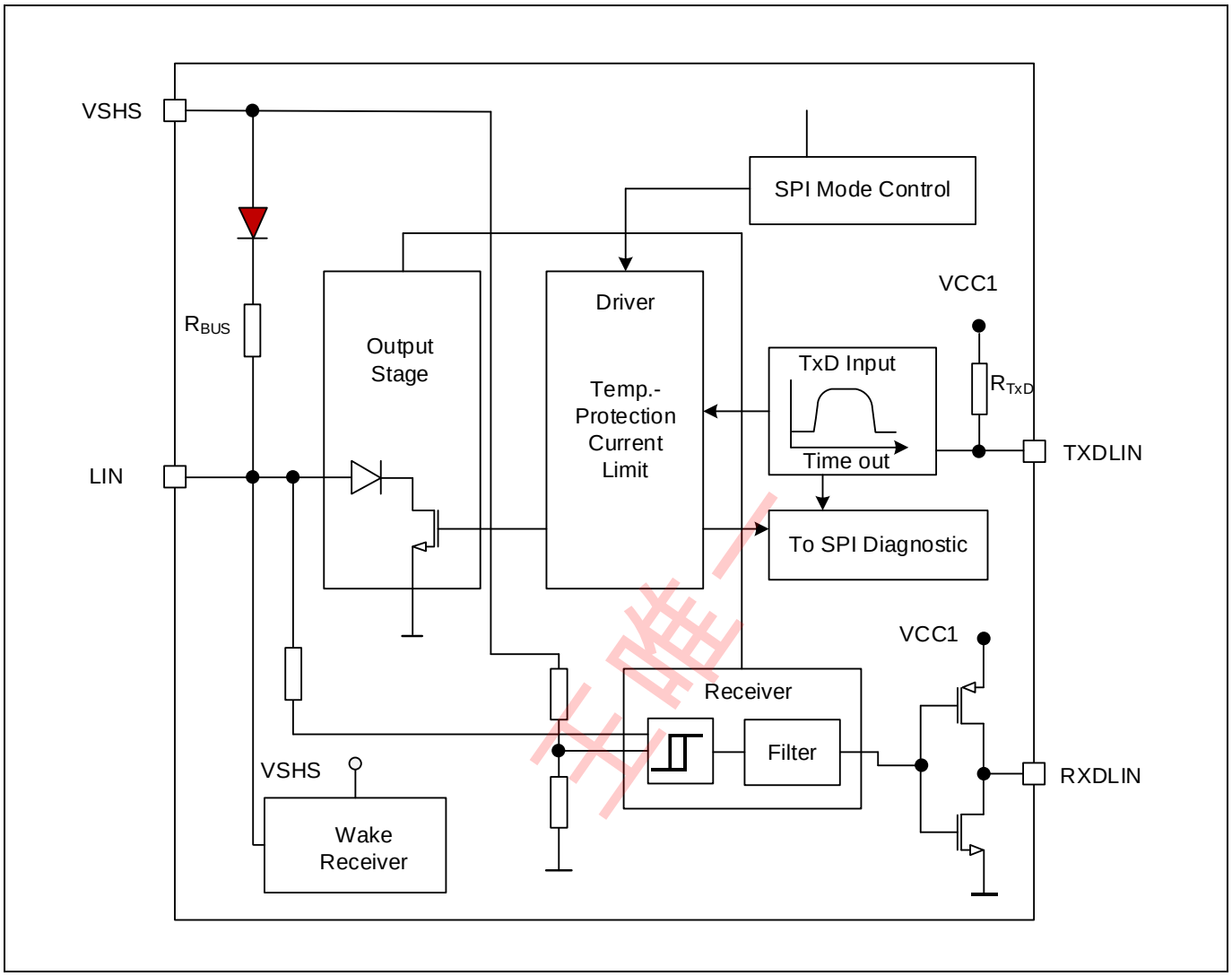


Figure 37 Block Diagram

11.1.1 LIN Specifications

The LIN network is standardized by international regulations.

The device is compliant to the physical layer standard LIN 2.2/ISO 17987-4 and SAE J2602-2. The SAE J2602-2 standard differs from the LIN 2.2/ISO 17987-4 standard mainly by the lower data rate (10.4 kbit/s).

11.2 Functional Description

The LIN Bus is a single-wire, bi-directional communication interface used in in-vehicle networks. The LIN transceiver integrated in the GD33AP236x devices provides the physical layer interface between the microcontroller and the LIN Bus.

Digital output data from the microcontroller are transmitted to the LIN Bus through the TXD input pin. The TXD data stream is converted into a LIN Bus signal with an optimized slew rate, effectively minimizing electromagnetic emissions (EME) within the LIN network.

Incoming data from the LIN Bus are received and forwarded to the microcontroller via the RXD output pin. The receiver incorporates an integrated filter network that suppresses noise on the LIN Bus and enhances the electromagnetic immunity (EMI) performance of the transceiver.

According to LIN 2.2 / ISO 17987-4, two logical states are defined on the LIN Bus.

Each LIN network consists of a master node and one or more slave nodes. For master node configuration, the GD33AP236x requires a resistor (1 kΩ) and a reverse diode connected between the LIN Bus and the VSHS power supply.

The LIN transceiver modes are controlled via SPI and **LIN2** configuration bits.

Figure 38 shows the possible transceiver mode transitions when changing the SBC mode.

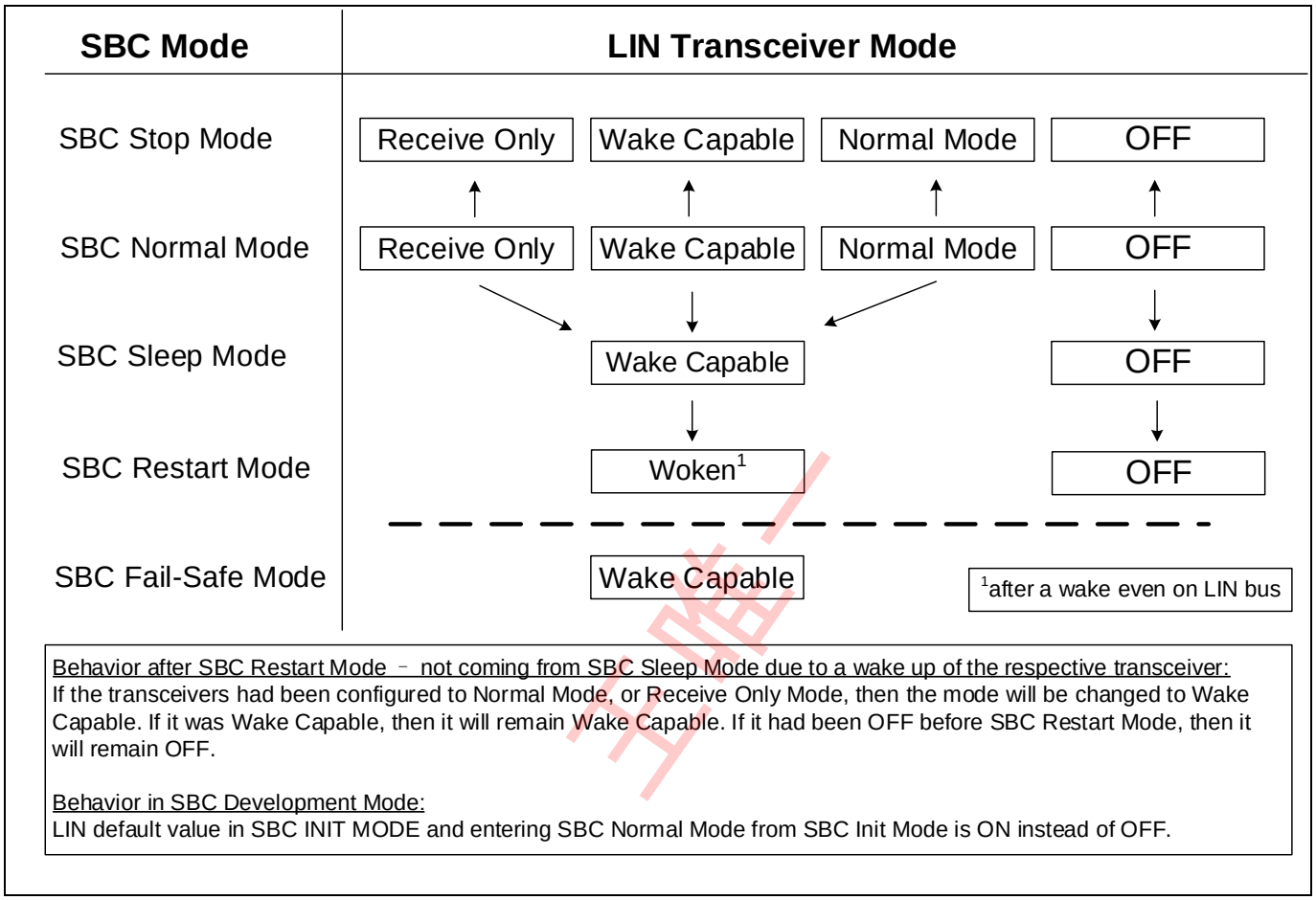


Figure 38 LIN Mode Control Diagram

11.2.1 LIN OFF Mode

The LIN OFF Mode is the default state after the power-up of the SBC. This mode is available in all SBC operating modes and is intended to completely disable LIN activity when LIN communication is not required. In LIN OFF Mode, any wake-up event occurring on the LIN bus is ignored.

11.2.2 LIN Normal Mode

The LIN transceiver can be enabled via SPI when the SBC operates in SBC Normal Mode. LIN Normal Mode is designed for standard data transmission and reception within the LIN network. This mode is available in both SBC Normal Mode and SBC Stop Mode.

Transmission

The TXDLIN input of the SBC receives the transmit signal from the microcontroller. The bus driver converts this signal and drives the LIN output stage, transferring the data onto the LIN bus line.

Enabling Sequence

Before initiating communication, the LIN transceiver requires an enable time ($t_{LIN,EN}$). Data transmission on the bus can only occur after this enable time has elapsed. If the TXDLIN signal is pulled LOW before the enable time is completed, it must be returned to HIGH (recessive) until the activation period finishes.

Only the next dominant bit following the enable time will be successfully transmitted onto the LIN bus.

Figure 39 shows different scenarios and explanations for LIN enabling.

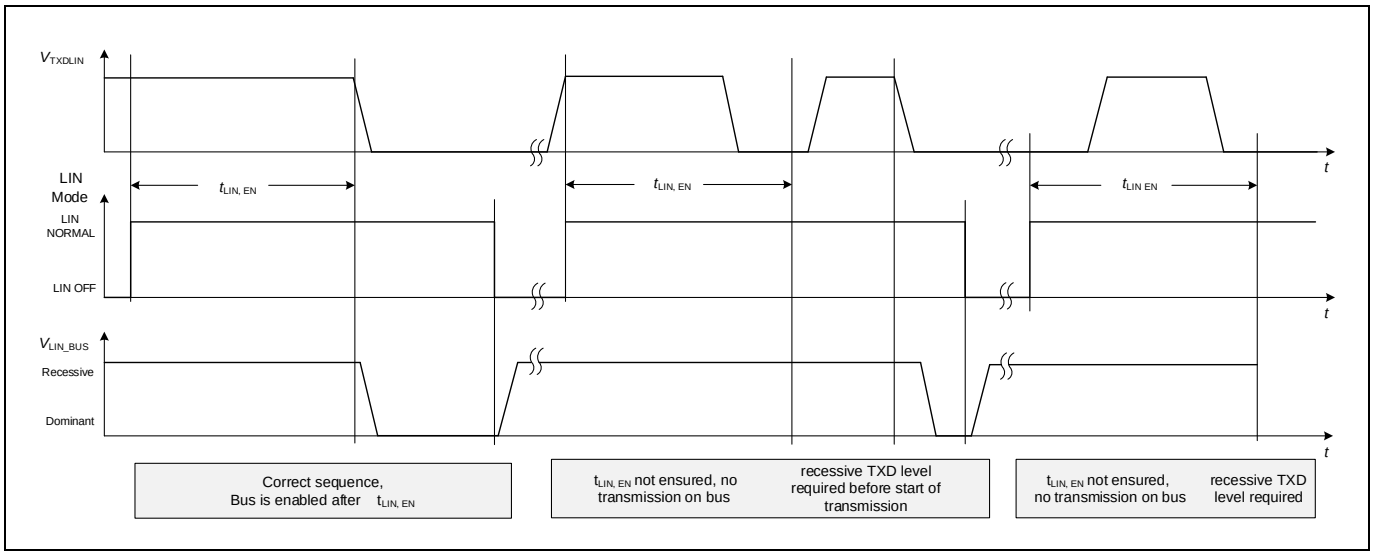


Figure 39 LIN Transceiver Enabling Sequence

Reduced Electromagnetic Emission

To reduce electromagnetic emissions (EME), the bus driver controls LIN slopes symmetrically. The configuration of the different slopes is described in **Chapter 11.2.8**.

Reception

Analog LIN bus signals are converted into digital signals at RXD via the differential input receiver.

11.2.3 LIN Receive Only Mode

In LIN Receive Only Mode (RXD-only), the driver stage of the LIN transceiver is deactivated, while data reception from the LIN bus remains enabled. This mode can be selected via SPI command and is available in both SBC Normal Mode and SBC Stop Mode.

11.2.4 LIN Wake Capable Mode

The LIN Wake Capable Mode is used to monitor bus activity and can be activated via SPI programming when the SBC operates in Stop, Sleep, Restart, or Normal Mode. It is also automatically entered in SBC Fail-Safe Mode. A wake-up event is detected when a recessive-to-dominant transition on the LIN bus is followed by a dominant level lasting longer than $t_{WK,Bus}$, and then by a dominant-to-recessive transition. This final transition triggers the wake-up of the LIN transceiver. Upon a wake-up, the RXD_LIN pin is driven LOW to signal the microcontroller and remains LOW until the transceiver is switched to another LIN mode. After a wake event, the transceiver can be set to LIN Normal Mode to resume communication.

Rearming the transceiver for wake capability

After a bus wake-up event, the transceiver becomes active, but the LIN1/ **LIN2** mode bits remain set to wake capable (‘01’), keeping the RXD signal LOW. The wake-capable mode can be re-enabled in two ways:

- By toggling the transceiver mode, i.e., switching to LIN Normal, LIN Receive Only, or LIN OFF Mode, and then back to LIN Wake Capable Mode.
- Automatically, when the SBC transitions to Stop, Sleep, or Fail-Safe Mode, ensuring continuous wake-up capability.

Wake-Up in SBC Stop and SBC Normal Mode

In SBC Stop Mode, a wake-up event is indicated by both the INT output and the **WK_STAT_1** SPI register, and additionally by pulling RXDLIN LOW. The same signaling behavior applies in SBC Normal Mode. After detection, the microcontroller must manually switch the device to SBC Normal Mode, as no automatic transition occurs.

For functional safety, if the watchdog was previously disabled, it will be automatically re-enabled after a bus wake event in SBC Stop Mode (if the bit **WD_EN_WK_BUS** was configured HIGH).

Wake-Up in SBC Sleep Mode

In SBC Sleep Mode, a wake-up can occur through a LIN message when the dominant level duration exceeds $t_{WK,Bus}$. This wake-up automatically transitions the SBC into Restart Mode, and subsequently to Normal Mode. During this process, the corresponding RXD pin is pulled LOW to notify the microcontroller. The microcontroller can then read the wake source from the **WK_STAT_1** register via SPI. No interrupt is generated when exiting Sleep Mode. After wake-up, the microcontroller can switch the LIN transceiver to LIN Normal Mode via SPI to initiate communication.

Table 25 Action due to a LIN BUS Wake-up

SBC Mode	SBC Mode after Wake	VCC1	INT	RXD
Normal Mode	Normal Mode	ON	LOW	LOW
Stop Mode	Stop Mode	ON	LOW	LOW
Sleep Mode	Restart Mode	Ramping Up	HIGH	LOW
Restart Mode	Restart Mode	ON	HIGH	LOW
Fail-Safe Mode	Restart Mode	Ramping up	HIGH	LOW

11.2.5 TXD Time-out Feature

If the TXD signal remains dominant for a duration longer than t >$t_{TxD\_LIN\_TO}$, the TXD time-out function temporarily deactivates the LIN transmitter output stage. During this condition, the transceiver output is forced into a recessive state to prevent the LIN bus from being blocked by a permanent LOW level on the TXD pin, which could occur due to a fault condition. When such a fault is detected, the event is recorded in the SPI status flags **LIN1_FAIL** and **LIN2_FAIL**. Once the dominant time-out condition is cleared, the LIN transmitter stage is automatically re-enabled, while the transceiver configuration remains unchanged.

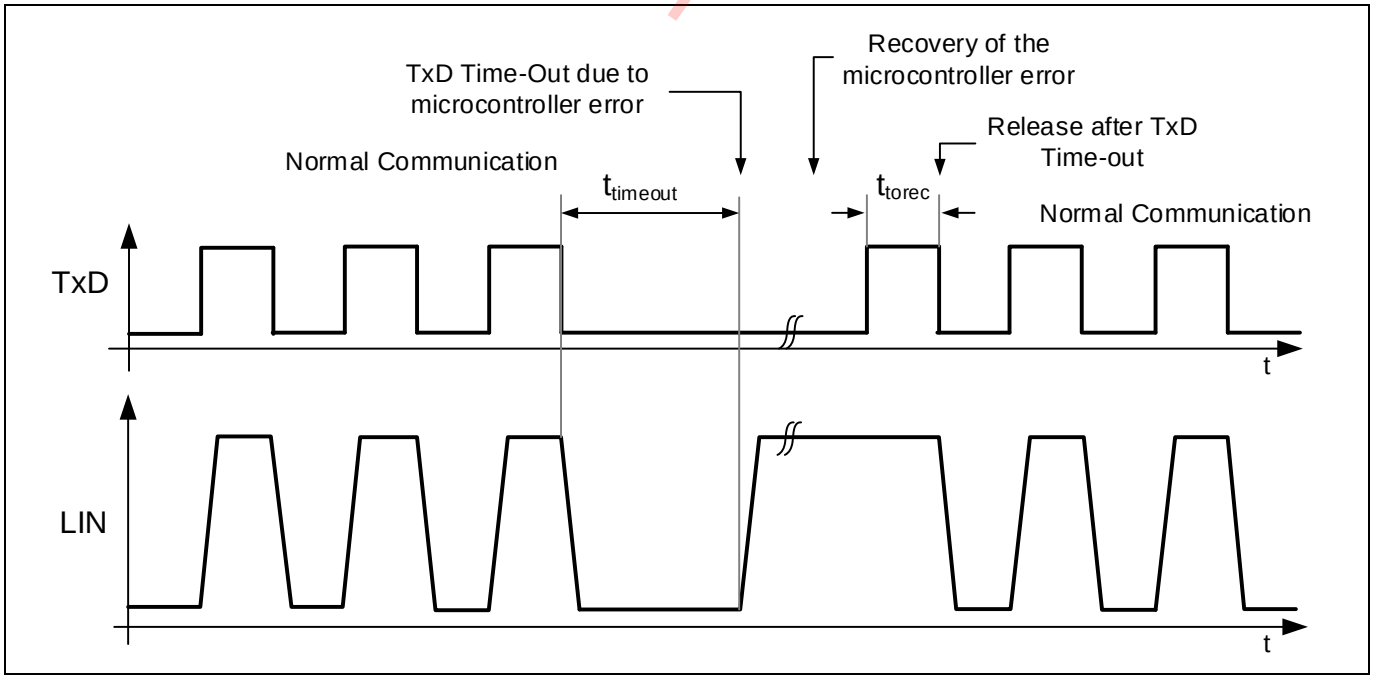


Figure 40 TXD Time-Out Function

11.2.6 Bus Dominant Clamping

If the LIN bus signal remains dominant for a duration longer than $t_{BUS\_LIN\_TO}$ while operating in LIN Normal Mode or LIN Receive Only Mode, a bus dominant clamping condition is detected. In such a case, the SPI status bits **LIN1_FAIL** and **LIN2_FAIL** are set to indicate the fault. The transceiver configuration remains unchanged.

11.2.7 Undervoltage Detection

When the supply voltage (VSHS) drops below the undervoltage detection threshold (VSHS < $V_{SHS,UVD}$), the GD33AP236x disables both the output and receiver stages. Once the supply voltage rises above the threshold (VSHS >$V_{SHS,UVD}$), the GD33AP236x resumes normal operation. Throughout this event, the transceiver configuration remains unchanged.

11.2.8 Slope Selection

The LIN transceiver supports two slope modes:

- LIN Low-Slope Mode for 10.4 kBaud communication
- LIN Normal-Slope Mode for 20 kBaud communication

The difference between these modes lies in the transmitter slew rate. In Low-Slope Mode, a reduced slew rate is used to minimize electromagnetic emissions (EME), ensuring compliance with SAE J2602 requirements. By default, the device operates in LIN Normal-Slope Mode. The Low-Slope Mode can be selected via the SPI bit **LIN_LSM**, which becomes effective when CSN transitions HIGH. Only the transmitter slope is modified, and this selection is available in SBC Normal Mode only.

11.2.9 Flash Programming via LIN

The device supports LIN-based flash programming, for example, programming another LIN slave node at data rates up to 115 kBaud. This feature is enabled by disabling the slope control mechanism through the SPI bit LIN_FLASH, which becomes effective once CSN goes HIGH. The SPI configuration bit can be set in SBC Normal Mode.

Note: It is recommended to perform flash programming only at nominal supply voltage VSHS = 13.5V to ensure stable data communication.

11.3 Electrical Characteristics

Table 26 Electrical Characteristics

V_{SHS} = 5.5 V to 18 V, T_j = -40 °C to +150 °C, RL = 500 Ω, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			
Receiver Output (RXD pin)							
HIGH Level Output Voltage	$V_{RXD,H}$	0.8 × V_{CC1}	–	–	V	I_{RXD} = -1.6 mA; V_{Bus} = V_{SHS}	
LOW Level Output Voltage	$V_{RXD,L}$	–	–	0.2 × V_{CC1}	V	I_{RXD} = 1.6 mA V_{Bus} = 0 V	
Transmission Input (TXD pin)							
HIGH Level Input Voltage	$V_{TXD,H}$	0.7 × V_{CC1}	–	–	V	Recessive State	
TXD Input Hysteresis	$V_{TXD,hys}$	–	0.5 × V_{CC1}	–	V	1)	
LOW Level Input Voltage	$V_{TXD,L}$	–	–	0.3 × V_{CC1}	V	Dominant State	
TXD Pull-up Resistance	R_{TXD}	20	40	80	kΩ	V_{TXD} = 0 V	
LIN Bus Receiver (LIN Pin)							

Receiver Threshold Voltage, Recessive to Dominant Edge	$V_{Bus,rd}$	0.4 × V_{SHS}	0.45 × V_{SHS}	–	V		
Receiver Dominant State	$V_{Bus,dom}$	–	–	0.4 × V_{SHS}	V	LIN 2.2/ISO 17987-4 Param 17	
Receiver Threshold Voltage, Dominant to Recessive Edge	$V_{Bus,dr}$	–	0.55 × V_{SHS}	0.60 × V_{SHS}	V		
Receiver Recessive State	$V_{Bus,rec}$	0.6 × V_{SHS}	–	–	V	LIN 2.2/ISO 17987-4 Param 18	
Receiver Center Voltage	$V_{Bus,c}$	0.475 × V_{SHS}	0.5 × V_{SHS}	0.525 × V_{SHS}	V	LIN 2.2/ISO 17987-4 Param 19 6 V < V_{SHS} < 18 V	
Receiver Hysteresis	$V_{Bus,hys}$	0.07 × V_{SHS}	0.1 × V_{SHS}	0.175 × V_{SHS}	V	$V_{bus,hys}$ = $V_{bus,dr}$ - $V_{bus,rd}$ LIN 2.2/ISO 17987-4 Param 20	
Wake-up Threshold Voltage	$V_{Bus,wk}$	0.40 × V_{SHS}	0.5 × V_{SHS}	0.6 × V_{SHS}	V	–	
Dominant Time for Bus Wake-up	$t_{WK,Bus}$	30	–	150	µs	2)	

Table 26 Electrical Characteristics (cont'd)

V_{SHS} = 5.5 V to 18 V, T_j = -40 °C to +150 °C, RL = 500 Ω, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			
LIN Bus Transmitter (LIN Pin)							
Bus Serial Diode Voltage Drop	$V_{serdiode}$	0.4	0.7	1.0	V	1) V_{TXD} = VCC1; LIN 2.2/ISO 17987-4 Param 21	
Bus Recessive Output Voltage	$V_{BUS,ro}$	0.8 × V_{SHS}	–	V_{SHS}	V	V_{TXD} = HIGH Level	
Bus Short Circuit Current	$I_{BUS,sc}$	40	100	150	mA	V_{BUS} = 18 V; LIN 2.2/ISO 17987-4 Param 12	
Leakage Current Loss of Ground	$I_{BUS,lk1}$	-1000	-450	20	µA	V_{SHS} = 12 V = GND; 0 V < V_{BUS} < 18 V; LIN 2.2/ISO 17987-4 Param 15	
Leakage Current Loss of Battery	$I_{BUS,lk2}$	–	–	20	µA	V_{SHS} = 0 V; V_{BUS} = 18 V; LIN 2.2/ISO 17987-4 Param 16	

Leakage Current Driver Off	$I_{BUS,lk3}$	-1	–	–	mA	V_{SHS} = 18 V; V_{BUS} = 0 V; LIN 2.2/ISO 17987-4 Param 13	
Leakage Current Driver Off	$I_{BUS,lk4}$	–	–	20	µA	V_{SHS} = 8 V; V_{BUS} = 18 V; LIN 2.2/ISO 17987-4 Param 14	
Bus Pull-up Resistance	R_{BUS}	20	30	47	kΩ	Normal Mode LIN 2.2/ISO 17987-4 Param 26	
LIN Input Capacitance	C_{BUS}		20	25	pF	1)	
Receiver propagation delay bus dominant to RXD LOW	$t_{d(L),R}$	–	1	6	µs	V_{CC} = 5 V; C_{RXD} = 20 pF; LIN 2.2/ISO 17987-4 Param 31	
Receiver propagation delay bus recessive to RXD HIGH	$t_{d(H),R}$	–	1	6	µs	V_{CC} = 5 V; C_{RXD} = 20 pF; LIN 2.2/ISO 17987-4 Param 31	
Receiver delay symmetry	$t_{sym,R}$	-2	–	2	µs	$t_{sym,R} = t_{d(L),R} - t_{d(H),R}$; LIN 2.2/ISO 17987-4 Param 32	

Table 26 Electrical Characteristics (cont'd)

V_{SHS} = 5.5 V to 18 V, T_j = -40 °C to +150 °C, RL = 500 Ω, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			
LIN Transceiver Enabling Time	$t_{LIN,EN}$	8	13	18	µs	2)CSN = HIGH to first valid transmitted TXD dominant	
Bus Dominant Time Out	$t_{BUS\_LIN\_TO}$	16	20	24	ms	1)2)	
TXD Dominant Time Out	$t_{TxD\_LIN\_TO}$	16	20	24	ms	1)2)V_{TXD} = 0 V	
TXD Dominant Time Out Recovery Time	t_{torec}	5	10	14	µs	1)2)	
Duty Cycle D1 (For worst case at 20 kbit/s) LIN 2.2/ISO 17987-4 Normal Slope	D1	0.396	–	–		3) TH_{Rec}(max) = 0.744 × V_{SHS}; TH_{Dom} (max) = 0.581 × V_{SHS}; V_{SHS} = 7.0 … 18 V; t_{bit} = 50 µs; D1 = $t_{bus\_rec(min)}$/2 t_{bit}; LIN 2.2/ISO 17987-4 Param 27	

Duty Cycle D2 (for worst case at 20 kbit/s) LIN 2.2/ISO 17987-4 Normal Slope	D2	–	–	0.581		3)TH_{Rec}(min.) = 0.422 × V_{SHS}; TH_{Dom}(min.) = 0.284 × V_{SHS}; V_{SHS} = 7.6 … 18 V; t_{bit} = 50 µs; D2 = $t_{bus\_rec(max)}$/2 t_{bit}; LIN 2.2/ISO 17987-4 Param 28	
Duty Cycle D3 (for worst case at 10.4 kbit/s) SAE J2602 Low Slope	D3	0.417	–	–		3)TH_{Rec}(max) = 0.778 × V_{SHS} TH_{Dom}(max) = 0.616 × V_{SHS}; V_{SHS} = 7.0 … 18 V; t_{bit} = 96 µs; D3 = $t_{bus\_rec(min)}$/2 t_{bit}; LIN 2.2/ISO 17987-4 Param 29	
Duty Cycle D4 (for worst case at 10.4 kbit/s) SAE J2602 Low Slope	D4	–	–	0.590		3)TH_{Rec}(min.) = 0.389 × V_{SHS}; TH_{Dom}(min.) = 0.251 × V_{SHS}; V_{SHS} = 7.6 … 18 V; t_{bit} = 96 µs; D4 = $t_{bus\_rec(max)}$/2 t_{bit}; LIN 2.2/ISO 17987-4 Param 30	

1) Not subject to production test, specified by design.
2) Not subject to production test, tolerance defined by internal oscillator tolerance
3) Bus load conditions concerning LIN 2.2/ISO 17987-4 C_{LIN}, R_{LIN} = 1 nF, 1 kΩ / 6.8 nF, 660 Ω/ 10 nF, 500 Ω

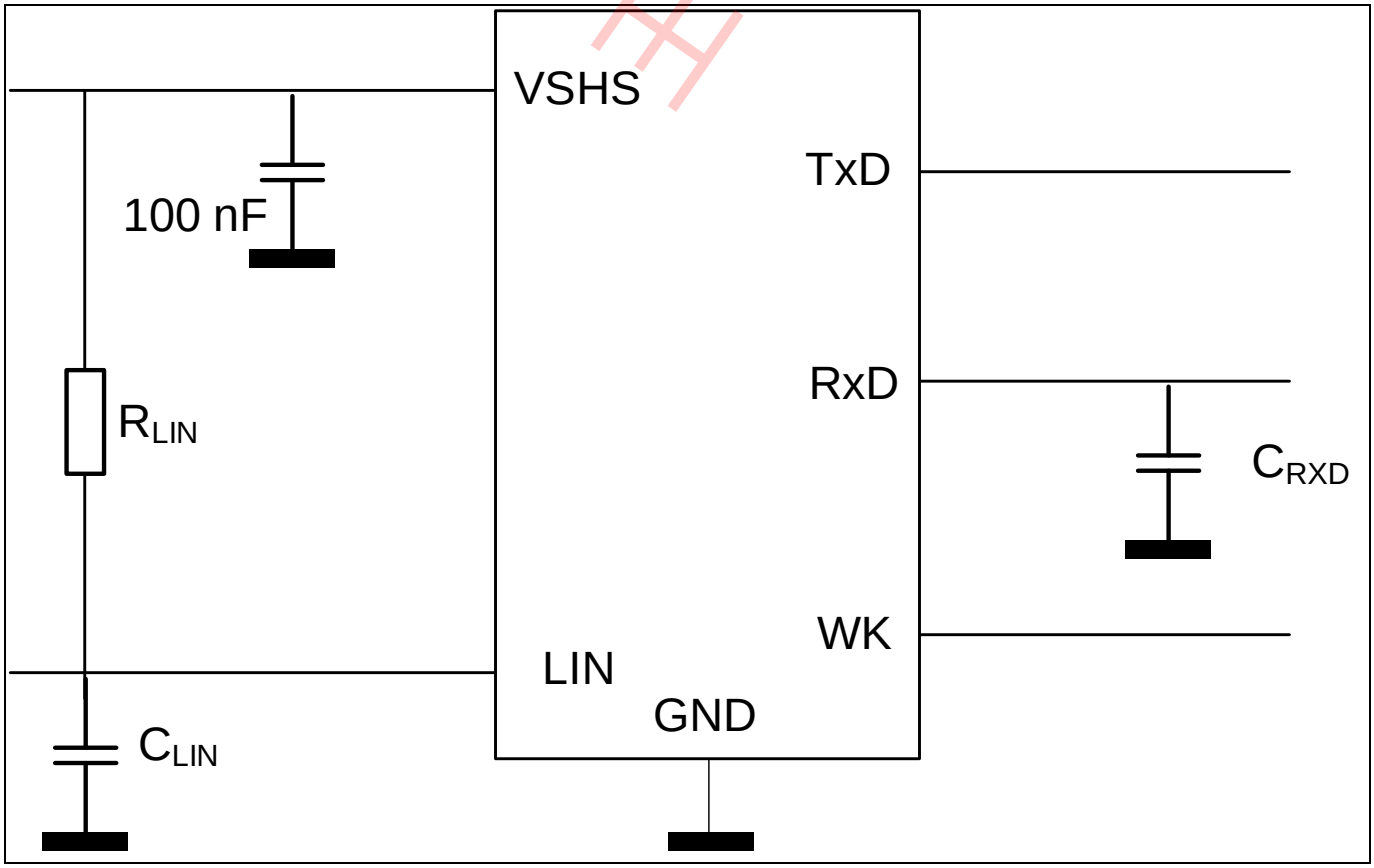


Figure 41 Simplified Test Circuit for Dynamic Characteristics

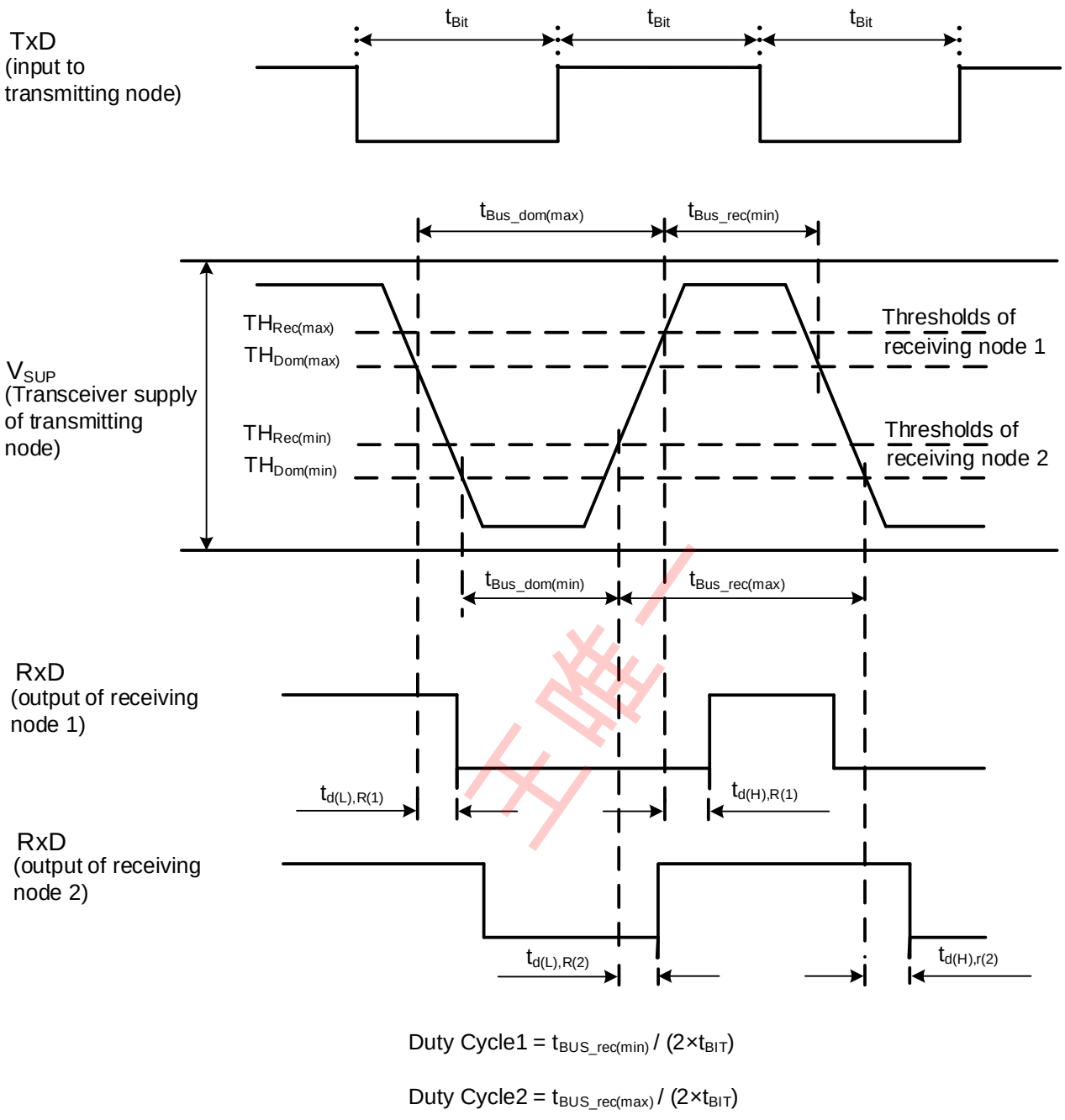


Figure 42 Timing Diagram for Dynamic Characteristics

12 Wake and Voltage Monitoring Inputs

12.1 Block Description

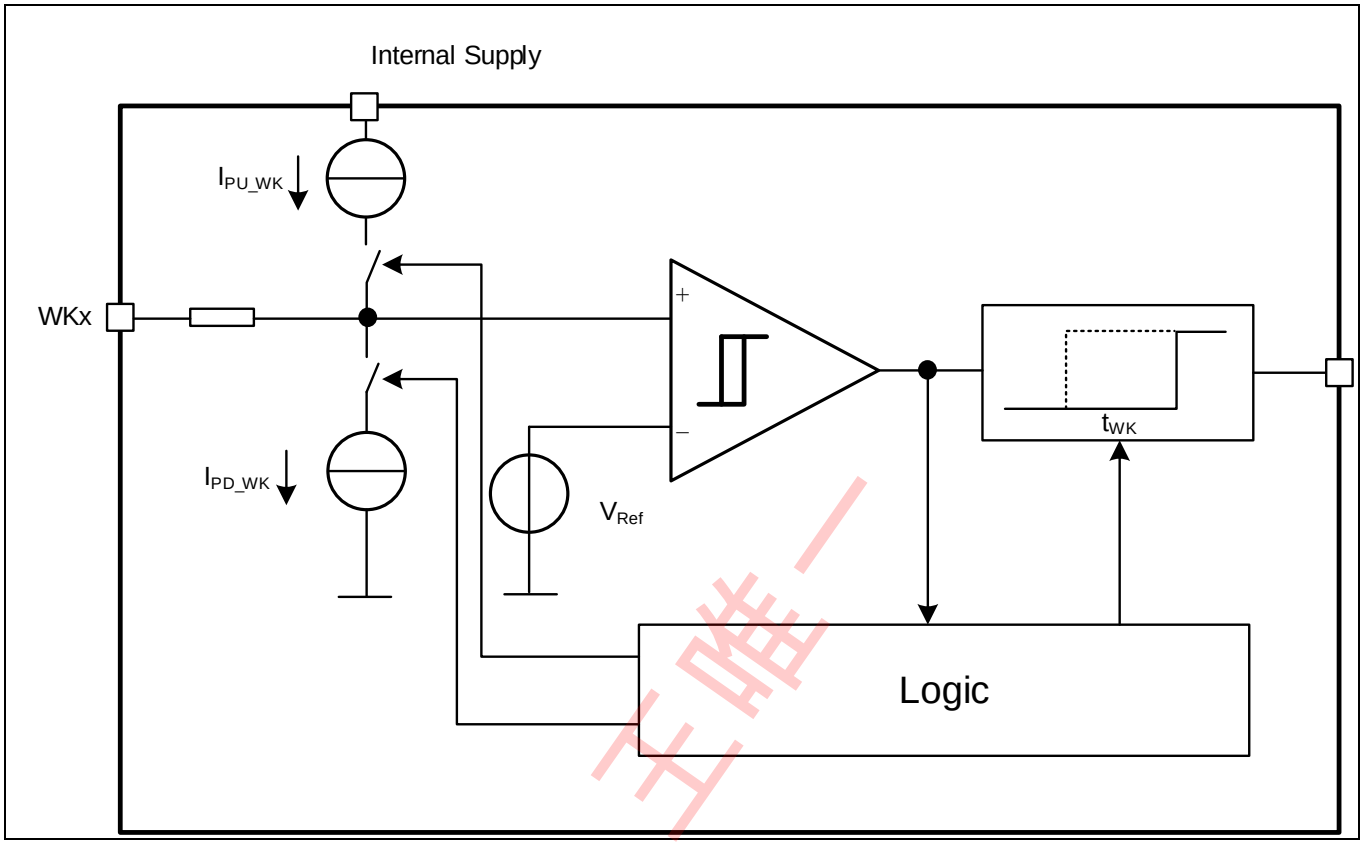


Figure 43 Wake Input Block Diagram

Features

- Three High-Voltage Inputs with a typical threshold voltage of 2.5 V, providing flexible signal detection for external wake sources.
- Alternate Measurement Function enabling high-voltage sensing via WK1 and WK2, allowing diagnostic or monitoring applications.
- Wake-Up Capability supporting transition from low-power modes (e.g., SBC Stop Mode) to active operation upon valid wake signal detection.
- Edge-Sensitive Wake Detection, capable of recognizing both LOW-to-HIGH and HIGH-to-LOW signal transitions for enhanced responsiveness.
- Configurable Pull-Up and Pull-Down Current Sources controlled via SPI interface, enabling precise adaptation to external circuit conditions.
- Selectable Static or Cyclic Sense Configuration, programmable to operate with TIMER1 and TIMER2 for periodic signal evaluation.
- In SBC Normal Mode and SBC Stop Mode, the WK pin level can be read via SPI even when the corresponding WK input is not enabled as a wake source, ensuring continuous system monitoring capability.

12.2 Functional Description

The wake input pins (WK1, WK2) are edge-sensitive digital inputs with a typical switching threshold of 2.5 V. Both signal transitions — HIGH to LOW and LOW to HIGH — are detected by the System Basis Chip (SBC).

Depending on the device operating mode, this detection results in either:

- Interrupt generation in SBC Normal Mode and SBC Stop Mode, or
- Device wake-up from SBC Sleep Mode or SBC Fail-Safe Mode.

Two different wake detection modes can be configured via the SPI interface:

- Static Sense Mode: WK inputs remain continuously active for immediate wake detection.
- Cyclic Sense Mode: WK inputs are periodically activated for a defined time window (refer to **Chapter 5.2.1**).

To suppress false wake-up events caused by transient signals or EMC disturbances, two filter times — 16 µs and 64 µs — can be selected in Static Sense Mode.

The filter time (t_{FWK1}, t_{FWK2}) is initiated when the input voltage crosses the switching threshold. A valid wake signal is recognized only if the input level remains stable and does not cross the threshold again during the selected filter period.

Figure 44 shows a typical wake-up timing and parasitic filter.

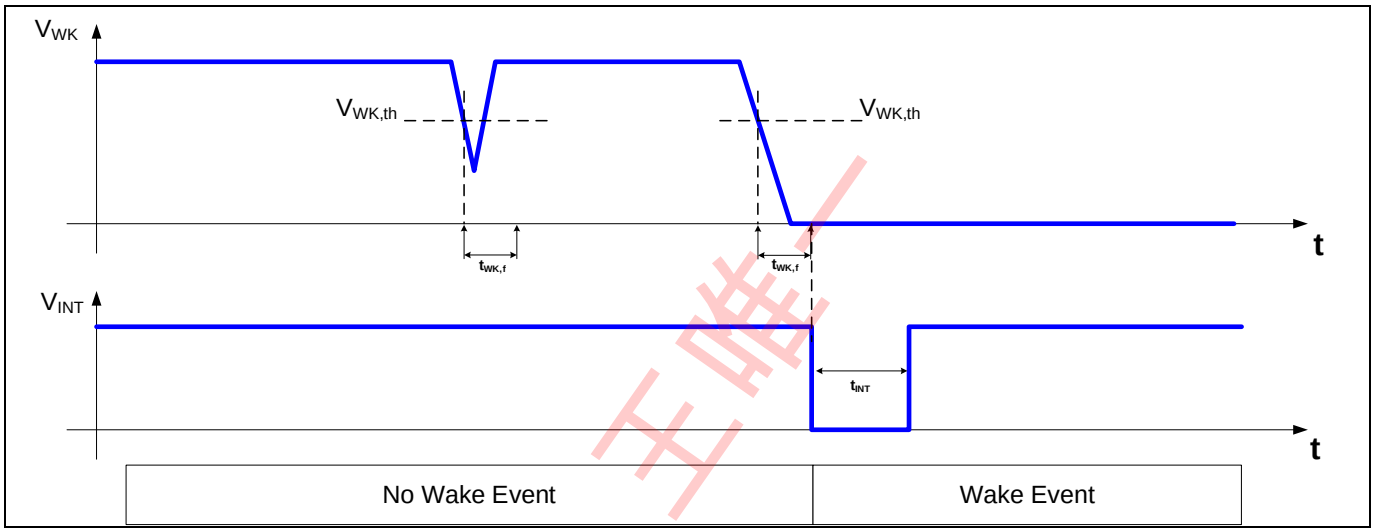


Figure 44 Wake-up Filter Timing for Static Sense

The wake-up capability of each WK pin can be enabled or disabled via an SPI command in the **WK_CTRL_2** register.

The wake source corresponding to a wake event triggered by any WKx pin can be read in the **WK_STAT_1** register, using the bits WK1_WU, WK2_WU, and WK3_WU for individual channel identification.

The actual voltage level of each WK pin (LOW or HIGH) can be monitored in SBC Normal Mode and SBC Stop Mode through the **WK_LVL_STAT** register.

During Cyclic Sense operation, this register provides the sampled voltage levels of the respective WK pins.

If FO2 and FO3 are configured as WK inputs in their alternate function (with a 16 µs static filter time), the corresponding wake events are indicated in the **WK_STAT_2** register.

12.2.1 Wake Input Configuration

To ensure defined and stable voltage levels at the internal comparator input, integrated current sources can be configured via the SPI register **WK_PUPD_CTRL**. Additionally, the wake detection modes, including the filter time settings, can be configured through the SPI register **WK_FLT_CTRL**. An example of the automatic switching configuration is illustrated in **Figure 45**.

Table 27 Pull-Up / Pull-Down Resistor

WKx_PUPD_1	WKx_PUPD_0	Current Sources	Note
0	0	no current source	WKx input is floating if left open (default setting)
0	1	pull-down	WKx input internally pulled to GND
1	0	pull-up	WKx input internally pulled to internal 5V supply

1	1	Automatic switching	If a high level is detected at the WKx input the pull-up source is activated, if low level is detected the pull down is activated.

Note: If there is no pull-up or pull-down configured on the WK input, then the respective input should be tied to GND or VS on board to avoid unintended floating of the pin and subsequent wake events

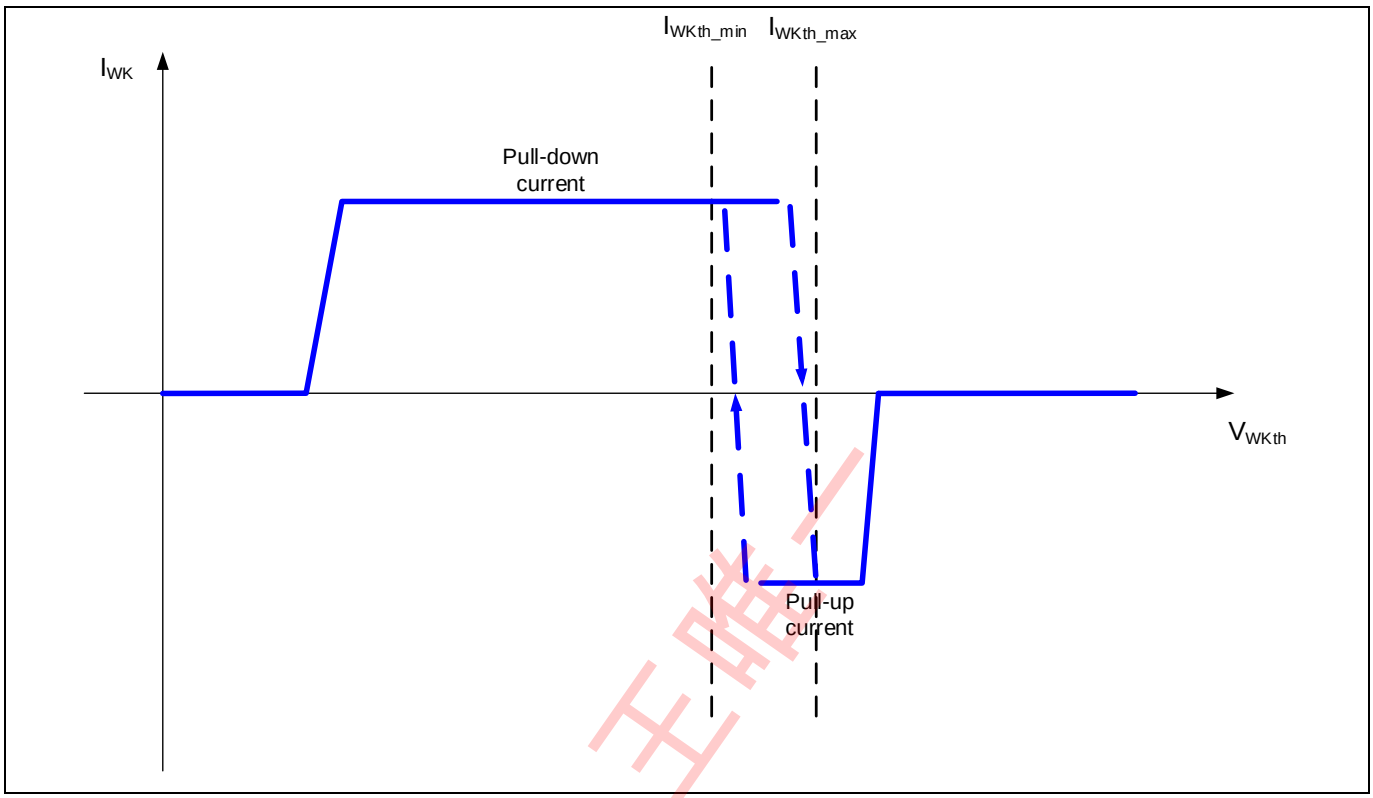


Figure 45 Illustration for Pull-Up/Down Current Sources with Automatic Switching Configuration

Table 28 Wake Detection Configuration and Filter Time

WKx_FLT_1	WKx_FLT_0	Filter Time	Description
0	0	Config A	static sense, 16µs filter time
0	1	Config B	static sense, 64µs filter time
1	0	Config C	Cyclic sense, Timer 1, 16µs filter time. Period, On-time configurable in register TIMER1_CTRL
1	1	Config D	Cyclic sense, Timer 2, 16µs filter time. Period, On-time configurable in register TIMER2_CTRL

Config A and B are intended for static sense with two different filter times.

Configuration C and Configuration D are intended for cyclic sense operation. When using these configurations, together with the selected filter settings, the corresponding timer must be assigned to one or more high-side (HS) outputs that supply the external circuitry connected to the respective WKx pin. For example, HS1 can be controlled by Timer 2 (HS1 = 010) and connected to WK3 through a switching circuit. For additional details, refer to **Chapter 5.2**.

12.2.2 Alternate Measurement Function with WK1 and WK2

12.2.2.1 Block Description

This function allows the measurement of a voltage, for example the unbuffered battery voltage, using the protected WK1 high-voltage (HV) input. The measured voltage is routed out through WK2. This enables, for instance, a voltage compensation for LED lighting applications by adjusting the duty cycle of the High-Side (HS) outputs. An external voltage divider must be implemented to provide the correct voltage level to the microcontroller A/D converter input. The function is available only in SBC Normal Mode and is disabled in all other modes to ensure low quiescent current operation. When enabled, this measurement function can replace the wake and level signaling capability of WK1 and WK2.

The advantages of this feature include:

- The signal is measured through a high-voltage input pin (WK1).
- No current flows through the resistor divider during low-power modes.

A simplified illustration of this functionality is provided in **Figure 65**.

12.2.2.2 Functional Description

By default, the measurement function is disabled. In this state, WK1 and WK2 operate with their standard wake and voltage level signaling functionality, and the switch S1 remains open (see **Figure 65**). The measurement function can be enabled via the SPI bit **WK_MEAS**.

When **WK_MEAS** = '1', the function becomes active and switch S1 is closed in SBC Normal Mode. In all other SBC modes, S1 remains open.When the measurement function is enabled:

- The pull-up and pull-down currents of WK1 and WK2 are disabled.
- The internal WK1 and WK2 signals are gated.
- The configurations of WK1 and WK2 in registers **WK_PUPD_CTRL**, **WK_FLT_CTRL**, and **WK_CTRL_2** are ignored, although register modification is still allowed.
- The **WK_STAT_1** and **WK_LVL_STAT** registers are not updated with respect to WK1 and WK2 inputs.

However, if WK1 or WK2 are individually configured as wake sources and an SBC Sleep Mode command is issued, the **SPI_FAIL** flag will be set, and the SBC will transition into SBC Restart Mode (see **Chapter 5.1** for details on wake functionality of WK1 and WK2).

Table 29 Differences between Normal WK Function and Measurement Function

Affected Settings/Modules for WK1 and WK2 Inputs	WK_MEAS = 0	WK_MEAS = 1
S1 configuration	'open'	'closed' in SBC Normal Mode, 'open' in all other SBC Modes
Internal WK1 & WK2 signal processing	Default wake and level signaling function, **WK_STAT_1**, **WK_STAT_2** are updated accordingly	'WK1...2 inputs are gated internally, **WK_STAT_1**, **WK_STAT_2** are not updated
WK1_EN, **WK2_EN**	Wake-up via WK1 and WK2 possible if bits are set	setting the bits is ignored and not prevented. If only **WK1_EN**, **WK2_EN** are set while trying to go to SBC Sleep Mode, then the **SPI_FAIL** flag will be set and the SBC will be changed into SBC Restart Mode.
WK_PUPD_CTRL	normal configuration is possible	no pull-up or pull-down enabled
WK_FLT_CTRL	normal configuration is possible	setting the bits is ignored and not prevented

Note: There is a diode in series to the switch S1 (not shown in the **Figure 65**), which will influence the temperature behavior of the switch.

12.3 Electrical Characteristics

Table 30 Electrical Characteristics

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			
WK1...WK3 Input Pin Characteristics							
Wake-up/monitoring threshold voltage	V_{WKth}	1.5	2.5	3.5	V	without external serial resistor R_S (with R_S: $\Delta V = I_{PD/PU} * R_S$); hysteresis included	
Threshold hysteresis	$V_{WKNth,hys}$	0.1	-	0.7	V	without external serial resistor R_S (with R_S: $\Delta V = I_{PD/PU} * R_S$);	
WK pin Pull-up Current	I_{PU_WK}	-20	-10	-3	µA	V_{WK_IN} = 3.5V	
WK pin Pull-down Current	I_{PD_WK}	3	10	20	µA	V_{WK_IN} = 1.5V	
Input leakage current	$I_{LK,I}$	-2		2	µA	0 V < V_{WK_IN} < 40V	
Drop Voltage across S1 switch	$V_{Drop,S1}$	–	1000	1100	mV	1) Drop Voltage between WK1 and WK2 when enabled for voltage measurement; I_{WK1} = 500µA; T_j = 25°C Refer to **Figure 46**	
Timing							
Wake-up filter time 1	t_{FWK1}	12	16	20	µs	2)SPI Setting	
Wake-up filter time 2	t_{FWK2}	50	64	80	µs	2)SPI Setting	

1) Not subject to production test; specified by design

2) Not subject to production test, tolerance defined by internal oscillator tolerance

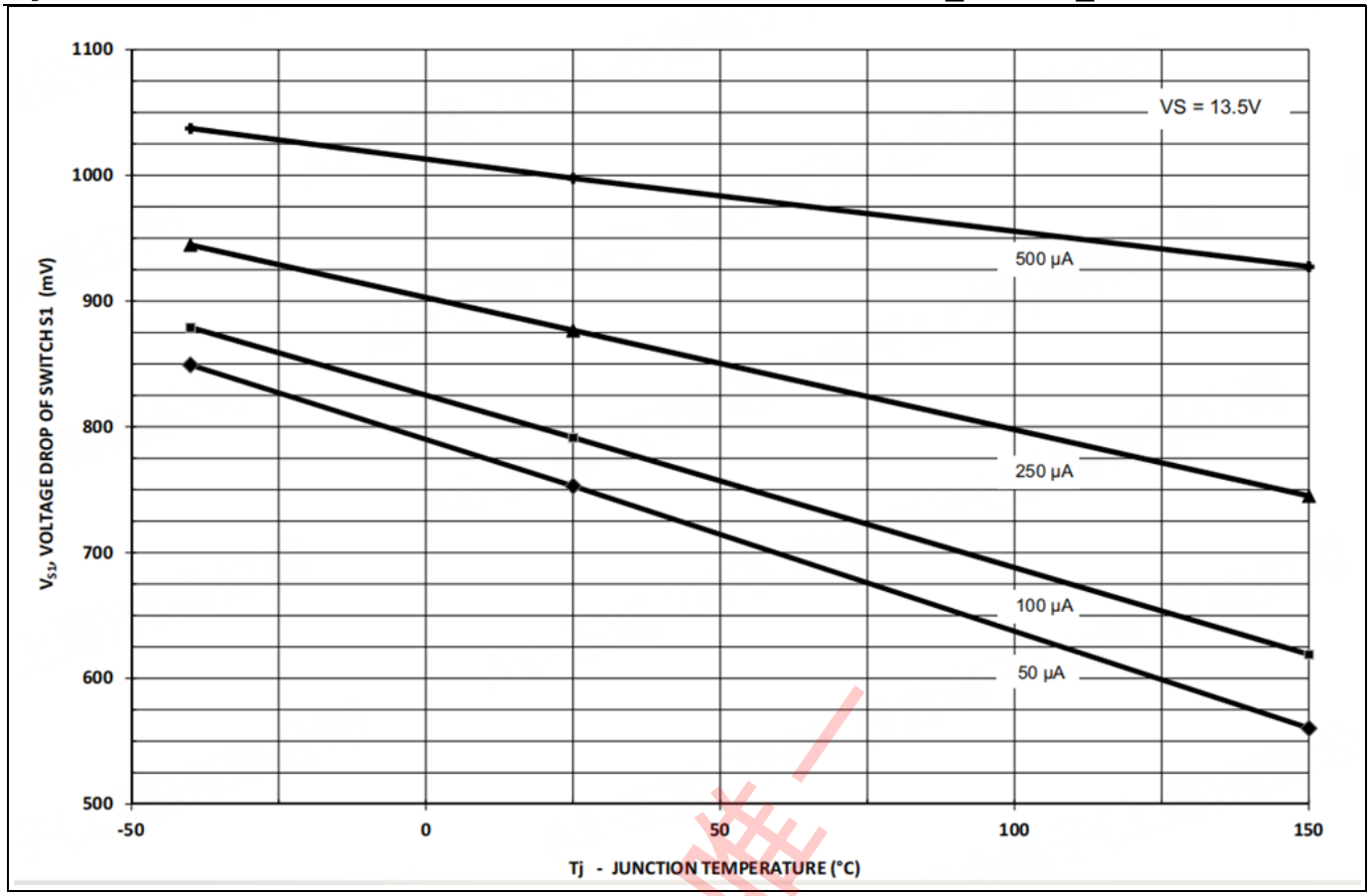


Figure 46 Typical Drop Voltage Characteristics of S1 (between WK1 & WK2)

13 Interrupt Function

13.1 Block and Functional Description

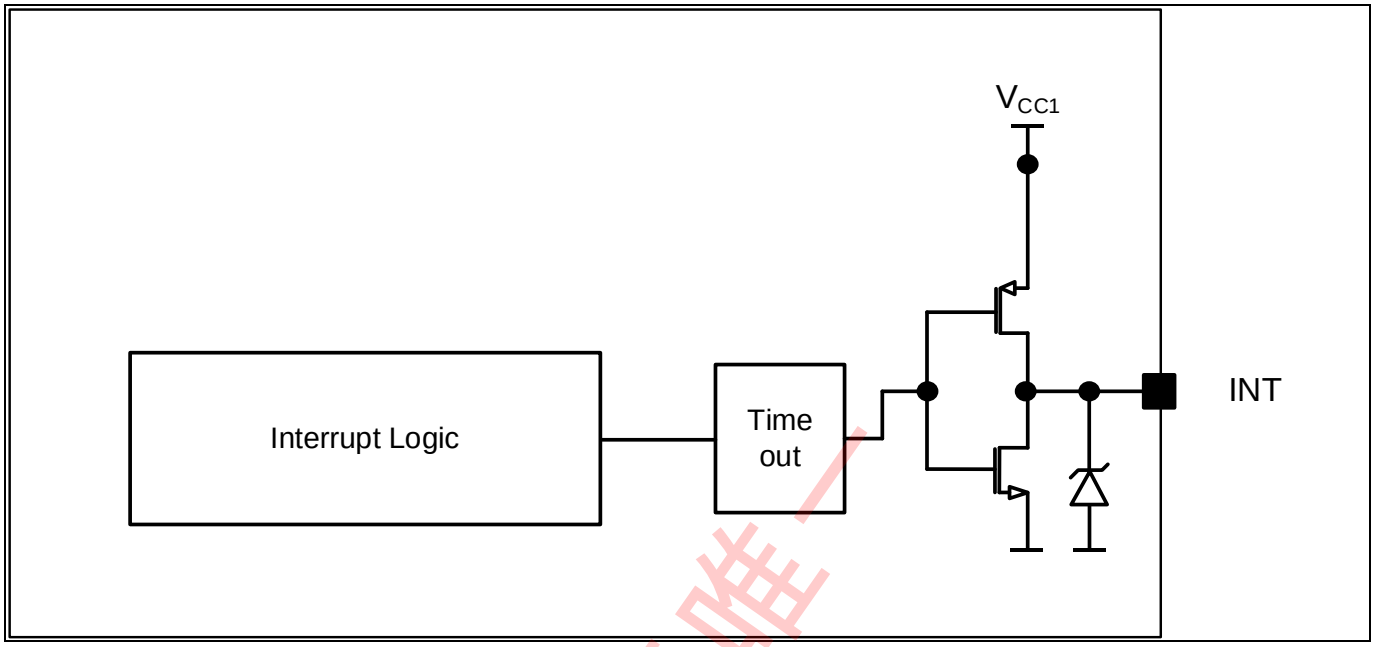


Figure 47 Interrupt Block Diagram

The interrupt function is used to signalize specific system events in real time to the microcontroller. The interrupt output stage is implemented as a push-pull driver, as illustrated in **Figure 47**. An interrupt event is triggered when a monitored condition occurs. The INT pin is then driven LOW (active low) for the defined duration t_{INT} in SBC Normal Mode and SBC Stop Mode, and it is released HIGH once t_{INT} has expired. The minimum HIGH time between two consecutive interrupts is t_{INTD}. An interrupt does not cause any SBC mode transition.

Two interrupt classes can be selected via the SPI bit **INT_ GLOBAL**:

- Class 1 (Wake Interrupt – **INT_ GLOBAL** = 0): All wake-up events stored in the wake status registers (**WK_STAT_1** and **WK_STAT_2**) generate an interrupt (default configuration). An interrupt is triggered only if the respective function is enabled as a wake source, including GPIOx when configured as a wake input. The CAN timeout signal (**CANTO**) is also treated as a wake source. The **CANTO_ MASK** bit has higher priority than **INT_ GLOBAL**, meaning **INT_ GLOBAL** is not considered for CANTO signalization.
- Class 2 (Global Interrupt – **INT_ GLOBAL** = 1): In addition to all wake-up events, any failure conditions stored in other status registers also generate an interrupt. The **WK_LVL_STAT** register does not generate interrupt requests.

Note: Errors that lead to SBC Restart or SBC Fail-Safe Mode (such as VCC1_UV, WD_FAIL, VCC1_SC, TSD2, FAILURE) are exceptions and do not trigger interrupt generation. Additionally, POR and DEV_STAT_x events do not generate interrupts.

An INT signal is also triggered when the SBC transitions to Stop Mode and pending bits remain uncleared in the **WK_STAT_1** or **WK_STAT_2** registers.

The SPI status registers are updated on every falling edge of the INT pulse.All interrupt events are latched in their corresponding status registers (except **WK_LVL_STAT**) until they are read and cleared via an SPI command. A second SPI read after clearing is optional but recommended to verify that no further interrupt condition remains. The interrupt timing behavior for Class 1 is illustrated in **Figure 48**. The behavior for Class 2 is identical.

During SBC Init Mode, the INT pin is also used to select the device hardware configuration (refer to **Chapter 5.1.1** for details).

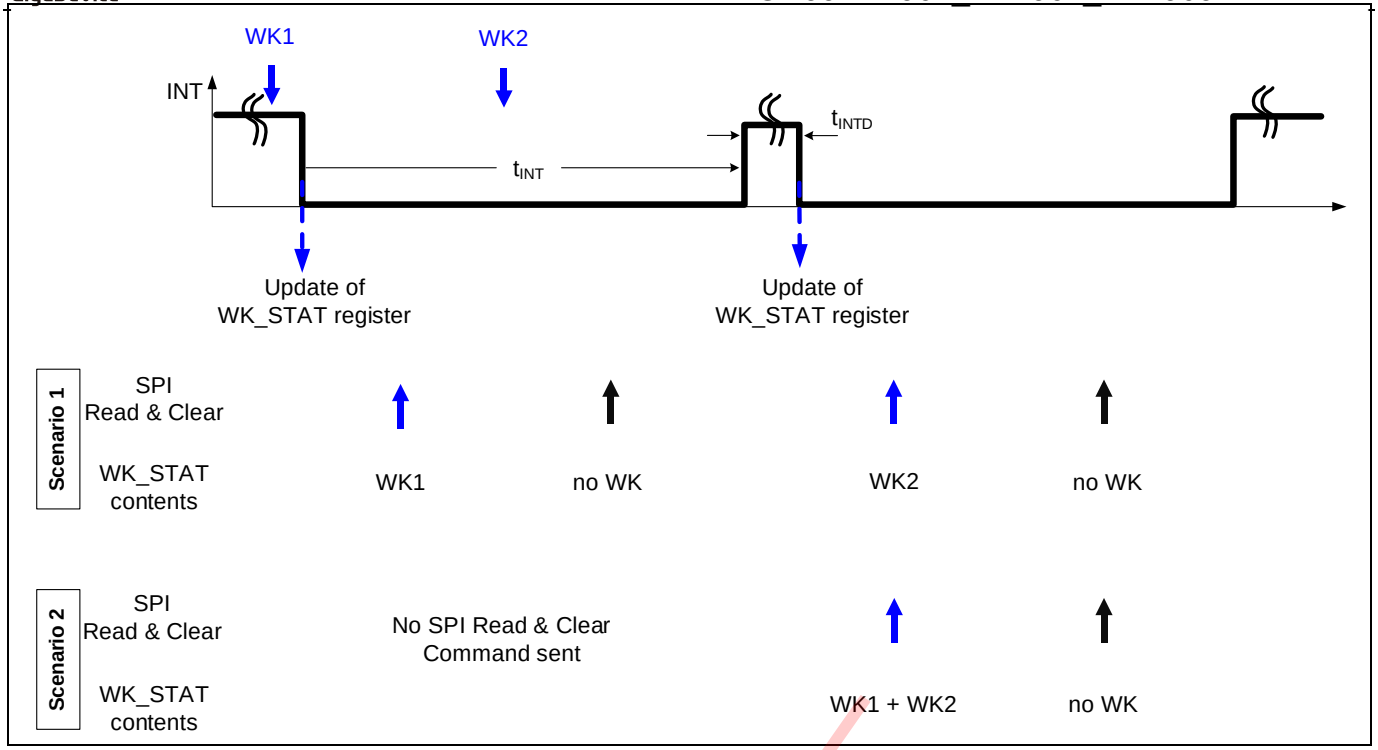


Figure 48 Interrupt Signalization Behavior

13.2 Electrical Characteristics

Table 31 Electrical Characteristics

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			
Interrupt Output; Pin INT							
INT High Output Voltage	$V_{INT,H}$	0.8 × V_{CC1}	–	–	V	1) I_{INT} = -1 mA; INT = OFF	
INT Low Output Voltage	$V_{INT,L}$	–	–	0.2 × V_{CC1}	V	1) I_{INT} = 1 mA; INT = ON	
INT Pulse Width	t_{INT}	80	100	120	µs	2)	
INT Pulse Minimum Delay Time	t_{INTD}	80	100	120	µs	2) between consecutive pulses	
Configuration Select; Pin INT							
Config Pull-down Resistance	R_{CFG}	180	250	350	kΩ	V_{INT} = 5 V	
Config Select Filter Time	t_{CFG_F}	5	10	14	µs	2)	

1) Output Voltage Value also determines device configuration during SBC Init Mode
2) Not subject to production test, tolerance defined by internal oscillator tolerance.

14 Fail Outputs

14.1 Block and Functional Description

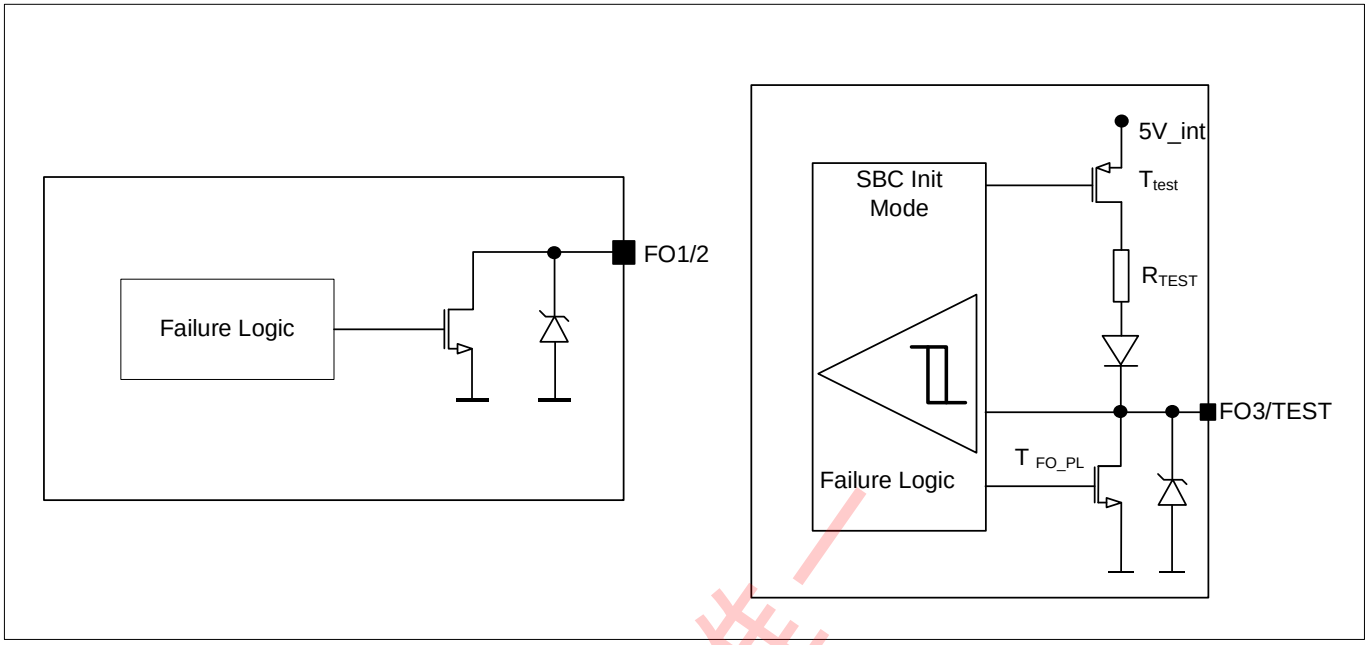


Figure 49 Simplified Fail Output Block Diagram for FO1/2 and for FO3/TEST

The Fail Outputs consist of a failure logic block and three open-drain outputs (FO1, FO2, FO3) with active-low signalization.

These outputs are activated under the following failure conditions:

- Watchdog trigger failure(For Config 3 & 4: after the second watchdog trigger failure, For Config 1 & 2: after the first watchdog trigger failure)
- Thermal shutdown (TSD2)
- VCC1 short circuit to GND
- VCC1 overvoltage, if the SPI bit **VCC1_OV_RST** is set
- Four consecutive VCC1 undervoltage events (refer to **Chapter 15.6** for details)

When any of these conditions occur, the SBC enters Fail-Safe Mode, except for certain watchdog-related exceptions depending on the selected configuration (see Chapter 5.1.1).

Activation of the Fail Outputs is indicated by the SPI bit **FAILURE** in the **DEV_STAT** register.

For testing purposes, the Fail Outputs can also be manually activated via SPI by setting the bit FO_ON. This bit operates independently from the failure logic. If no failure condition is present, the FO outputs can be deactivated via SPI, without requiring a successful watchdog trigger.

The entry into SBC Fail-Safe Mode due to a watchdog failure can be configured as described in **Chapter 5.1.1**.

To deactivate the Fail Outputs in SBC Normal Mode, the following conditions must be met: All failure conditions (e.g. TSD2, VCC1 short circuit) must no longer be present. The FAILURE bit must be cleared via SPI command.

In the case of a watchdog failure, the proper procedure to deactivate the Fail Outputs is:

- Perform a successful watchdog trigger, ensuring that **WD_FAIL** is cleared.
- Clear the **FAILURE** bit via SPI.

The **WD_FAIL** flag will also be cleared automatically when entering SBC Sleep Mode or SBC Fail-Safe Mode due to any other failure condition, or if the watchdog is disabled in SBC Stop Mode.

Note: The Fail Output pin is triggered for any of the failure conditions described above.However, no FAILURE indication is generated for the first watchdog failure when Config 2 is selected.

The three fail outputs (FO1, FO2, FO3) are activated simultaneously, each providing distinct output functionality as follows:

- FO1: Static fail output
- FO2: 1.25 Hz signal with 50% (typ.) duty cycle, typically used to generate an indicator signal
- FO3: 100 Hz PWM signal with 20% (typ.) duty cycle, typically used to generate a dimmed rear light derived from a brake light

Note: The FO3 duty cycle can be configured via SPI to 20%, 10%, 5%, or 2.5%, with 20% being the default value.The duty cycle configuration is accessible through the register **FO_DC**.

14.1.1 General Purpose I/O Functionality of FO2 and FO3 as Alternate Function

In applications where FO2 and FO3 are not utilized as Fail Outputs, these pins can alternatively be configured as high-voltage General Purpose I/O (GPIO) pins, which are related to the VSHS domain.

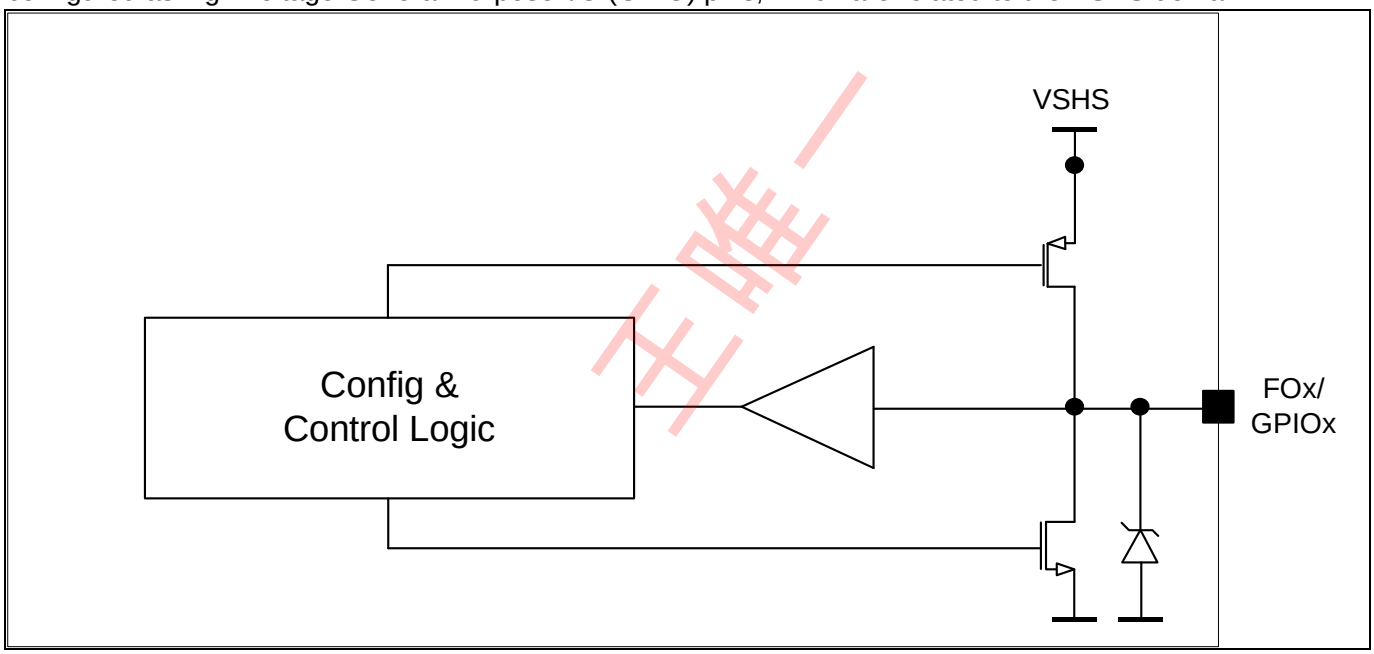


Figure 50 Simplified General Purpose I/O block diagram for FO2 and FO3/TEST

By default, the pins are configured as Fail Output (FO) pins. The configuration of these pins can be modified via the SPI register **GPIO_CTRL** to enable alternate functions as described below:

- Wake Inputs: The detection threshold ($V_{GPIOI,th}$) is similar to the WK inputs. The wake-up detection behavior is identical to that of the WKx pins. Wake events are stored and reported in the **WK_STAT_2** register.
- Low-Side Switches (LS): Capable of driving currents up to 10 mA (refer to $V_{GPIOI,L1}$). Each switch includes self-protection with respect to current limitation. No additional diagnostic function is implemented.
- High-Side Switches (HS): Capable of driving currents up to 10 mA (refer to $V_{GPIOI,H1}$). Each switch is self-protected against current limitation. No additional diagnostics are implemented.
- GPIO Mode: When configured as GPIO, the pin level is reflected in the **WK_LVL_STAT** register during SBC Normal and Stop Modes. The same feedback is also available when configured as LS or HS, providing a status indication of the respective state. GPIO2 shares functionality with the TEST level bit.

Table 32 describes the behavior of the FO/GPIO pins in their different configurations and SBC modes.

Table 32 Fail-Output and GPIO configuration behavior during the respective SBC Modes

FOx Configuration	SBC Normal Mode	SBC Stop Mode	SBC Sleep Mode	SBC Restart Mode	SBC Fail-Safe Mode
FOx (default)	configurable	fixed	fixed	active / fixed	active
OFF		OFF	OFF	OFF	OFF
Wake Input		wake capable	wake capable	wake capable	OFF
Low-Side		fixed	fixed	OFF	OFF
High-Side		fixed	fixed	OFF	OFF

Explanation of FO/GPIO states:

- Configurable: Settings can be changed in the corresponding SBC mode.
- Fixed: Settings remain as configured in SBC Normal Mode.
- Active: The FOx output is activated due to a failure condition, leading to SBC Restart or Fail-Safe Mode.

Restart Behavior:

The behavior during SBC Restart and Fail-Safe Mode as well as the transition to SBC Normal Mode is as follows:

The behavior during SBC Restart and Fail-Safe Mode, as well as the transition back to SBC Normal Mode, is defined as follows:

- If configured as Wake Input: The pin remains wake-capable during SBC Restart Mode, but is OFF while in Fail-Safe Mode. It resumes wake capability when leaving Restart Mode. The SPI register settings are not modified.
- If configured as Low-Side or High-Side Switch: These switches are disabled during Restart and Fail-Safe Mode. Upon leaving Restart Mode, the previous configuration is restored. The SPI register remains unchanged.
- If configured as Fail Output (FO): When activated due to a failure, the FO output remains active throughout Restart Mode and upon entering SBC Normal Mode. The SPI register is not modified.

Notes

1. To avoid unintended entry into SBC Development Mode, ensure that the FO3/TEST pin level is HIGH during device power-up and SBC Init Mode.
2. The FOx drivers are supplied via VS, whereas the GPIO High-Side switches (FO2, FO3/TEST) are supplied via VSHS.

14.2 Electrical Characteristics

Table 33 Electrical Characteristics

V_{SHS} = 5.5 V to 28 V; T_j = -40 °C to +150 °C; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			
Pin FO1							
FO1 low output voltage (active)	$V_{FO,L1}$	–	–	1.0	V	I_{FO} = 4mA	
FO1 high output current (inactive)	$I_{FO,H}$	0	–	2	µA	V_{FO} = 28V	
Pin FO2							

FO2 side indicator frequency	f_{FO2SI}	1.00	1.25	1.50	Hz	3)	
FO2 side indicator duty cycle	d_{FO2SI}	45	50	55	%	3)	

Pin FO3/TEST[2)]

Pull-up Resistance at pin FO3/TEST	R_{TEST}	2.5	5	10	kΩ	V_{TEST} =0V; SBC Init Mode	
TEST Input Filter Time	t_{TEST}	50	64	80	µs	3)	
FO3 pulsed light frequency	f_{FO3PL}	80	100	120	Hz	3)	
FO3 pulsed light duty cycle	d_{FO3PL}	16	20	24	%	3)4)default setting	

Alternate FO2...3

Electrical Characteristics: GPIO

GPIO low-side output voltage (active)	$V_{GPIOL,L1}$	–	–	1	V	I_{GPIO} = 10mA	
GPIO low-side output voltage (active)	$V_{GPIOL,L2}$	–	–	5	mV	5)I_{GPIO} = 50µA	
GPIO high-side output voltage (active)	$V_{GPIOH,H1}$	VSHS-1	–	–	V	I_{GPO} = -10mA	
GPIO high-side output voltage (active)	$V_{GPIOH,H2}$	VSHS-5	–	–	mV	5)I_{GPO} = -50µA	
GPIO input threshold voltage	$V_{GPIOI,th}$	1.5	2.5	3.5	V	6) hysteresis included	
GPIO input threshold hysteresis	$V_{GPIOI,hys}$	100	400	700	mV	5)	

Table 33 Electrical Characteristics (cont'd)

V_{SHS} = 5.5 V to 28 V; T_j = -40 °C to +150 °C; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			
GPIO low-side current limitation	$I_{GPIOL,max}$	10	–	30	mA	V_{GPIO} = 28V	
GPIO high-side current limitation	$I_{GPIOH,max}$	-45	–	-10	mA	V_{GPIO} = 0V	

1) The FOx drivers are supplied via VS. However, the GPIO HS switches (FO2, FO3/TEST) are supplied by VSHS
2) The external capacitance on this pin must be limited to less than 10nF to ensure proper detection of SBC Development Mode and SBC User Mode operation.
3) Not subject to production test, tolerance defined by internal oscillator tolerance.
4) The duty cyclic is adjustable via the SPI bits **FO_DC.**
5) Not subject to production test, specified by design.
6) Applies also for TEST voltage input level

15 Supervision Functions

15.1 Reset Function

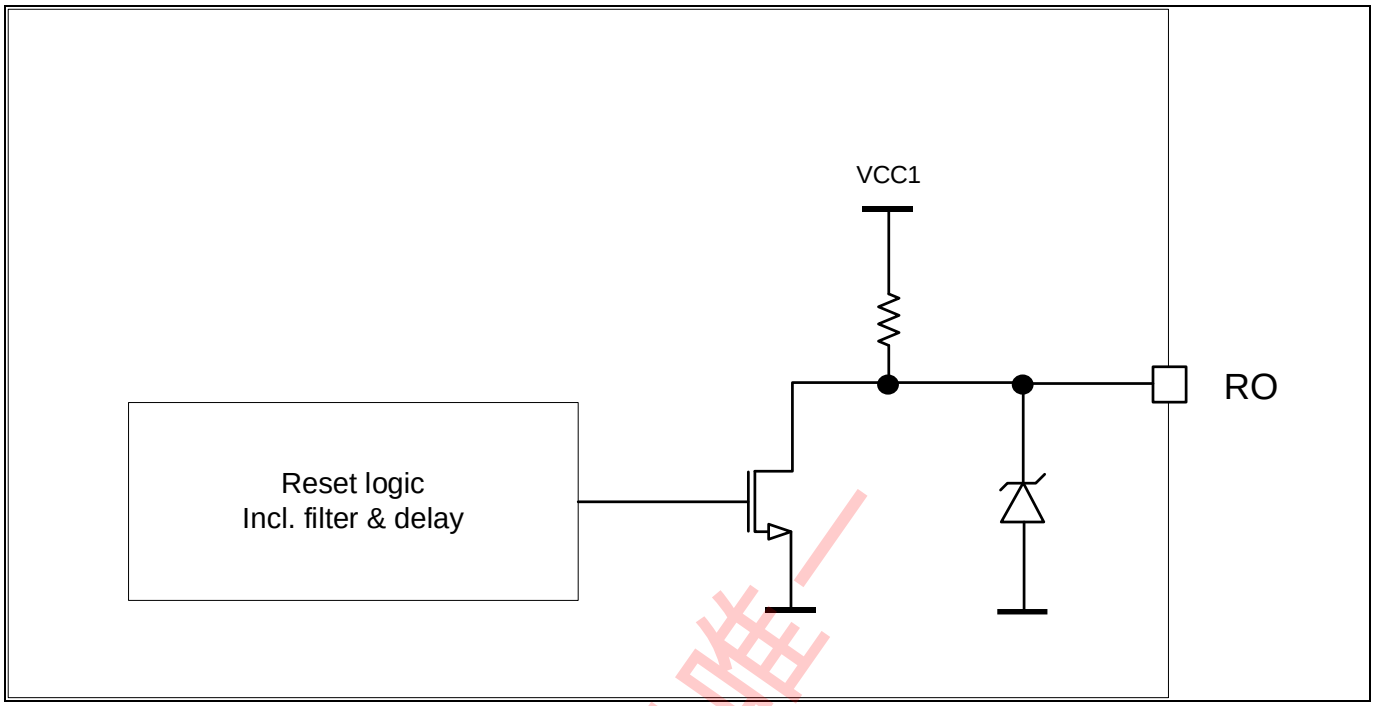


Figure 51 Reset Block Diagram

15.1.1 Reset Output Description

The Reset Output pin (RO) provides a reset indication to the microcontroller, for example, when the output voltage falls below the undervoltage threshold ($V_{RT1/2/3/4}$). In the event of a reset condition, the RO pin is pulled low after the filter time $\mathbf{t_{RF}}$ and remains low for the duration of the reset event, plus an additional reset delay time $\mathbf{t_{RD1}}$. When the SBC is first connected to the battery voltage, the reset signal initially stays LOW. Once the output voltage V_{cc1} reaches the default reset threshold $\mathbf{V_{RT1,r}}$, the RO output is released to HIGH after the reset delay time $\mathbf{t_{RD1}}$. A reset may also be triggered due to a watchdog failure. The reset threshold is configurable via SPI, with a default threshold of $\mathbf{V_{RT1,r}}$. The RO pin includes an integrated pull-up resistor. In the case of a reset trigger, the pin is pulled low for $\mathbf{V_{CC1}} \geq 1$ V and VS ≥ $\mathbf{V_{POR,f}}$ (refer to **Chapter 15.3**).

The timing behavior of the RO signal during VCC1 undervoltage and watchdog trigger events is illustrated in **Figure 52.**

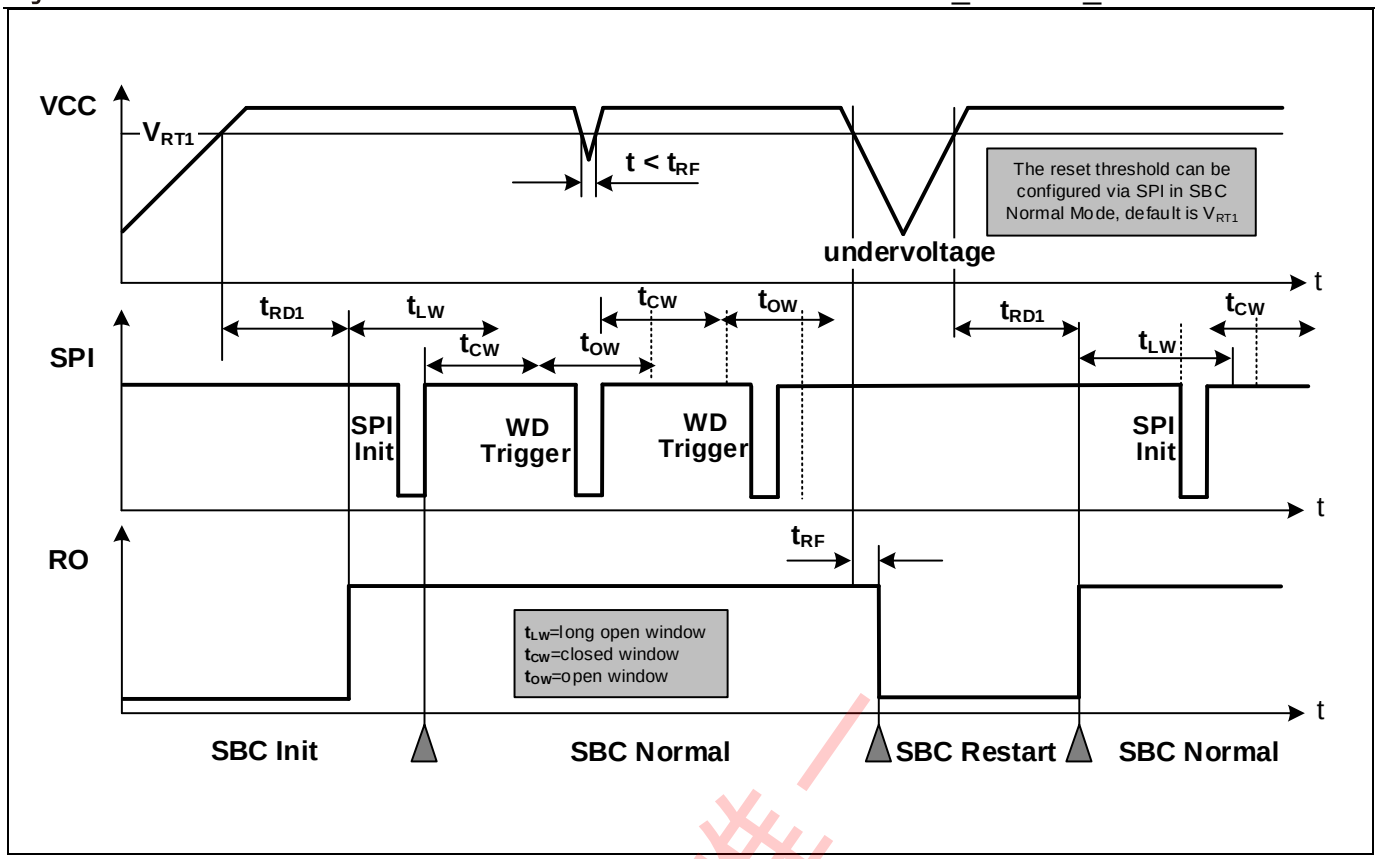


Figure 52 Reset Timing Diagram

15.1.2 Soft Reset Description

In SBC Normal Mode and SBC Stop Mode, it is possible to trigger an internal device reset via a SPI command in order to bring the SBC back to a defined state in case of failures. To execute a soft reset, the microcontroller must send a SPI command and set the **MODE** bits to '11' in the **M_S_CTRL** register. Once this command becomes valid, the SBC is returned to SBC INIT Mode, and all SPI registers are reset to their default values (refer to **Chapter 16.5** and **Chapter 16.6**).

Two different soft reset configurations can be selected via the SPI bit **SOFT_ RESET_RO**:

- The reset output (RO) is triggered when the soft reset is executed (default setting, the same reset delay time t_{RD1} applies).
- The reset output (RO) is not triggered when the soft reset is executed.

Note: The device must be in SBC Normal Mode or SBC Stop Mode when sending this command; otherwise, the command will be ignored.

15.2 Watchdog Function

The watchdog is used to monitor the software execution of the microcontroller and to trigger a reset if the microcontroller fails to serve the watchdog due to a software lock-up.

Two types of watchdog mechanisms are implemented and can be selected via the **WD_WIN** bit:

- Time-Out Watchdog (default value)
- Window Watchdog

The corresponding watchdog functions can be selected and programmed in SBC Normal Mode. The configuration remains unchanged in SBC Stop Mode.

Refer to **Table 34** for the correlation between SBC Modes and the respective watchdog modes.

Table 34 Watchdog Functionality by SBC Modes

SBC Mode	Watchdog Mode	Remarks

INIT Mode	Starts with Long Open Window	Watchdog starts with Long Open Window after RO is released
Normal Mode	WD Programmable	Window Watchdog, Time-Out watchdog or switched OFF for SBC Stop Mode
Stop Mode	Watchdog is fixed or OFF	
Sleep Mode	OFF	SBC will start with Long Open Window when entering SBC Normal Mode.
Restart Mode	OFF	SBC will start with Long Open Window when entering SBC Normal Mode.

The watchdog timing is programmed via a SPI command. Once the watchdog is programmed, the timer starts with the new setting, and the watchdog must be served accordingly. The watchdog is triggered by sending a valid SPI-write command to the watchdog configuration register. The trigger command becomes effective when the Chip Select input (CSN) switches to HIGH.

When entering from SBC Init Mode, SBC Restart Mode, or under certain conditions from SBC Stop Mode, the watchdog timer always starts with a long open window. This long open window (t_{LW} = 200 ms) allows the microcontroller to complete its initialization sequence before triggering the watchdog via SPI.

The watchdog timer period can be selected via the **WD_TIMER** bit field, ranging from 10 ms to 1000 ms. This configuration applies to both watchdog types. The following watchdog timer periods are available:

- WD Setting 1: 10 ms
- WD Setting 2: 20 ms
- WD Setting 3: 50 ms
- WD Setting 4: 100 ms
- WD Setting 5: 200 ms
- WD Setting 6: 500 ms
- WD Setting 7: 1000 ms

In the event of a watchdog-induced reset, the SBC enters Restart Mode or Fail-Safe Mode according to the configuration, and the SPI bits **WD_FAIL** are set. Once the Reset Output (RO) returns HIGH, the watchdog immediately starts with a long open window, and the SBC automatically transitions to Normal Mode.

In SBC Development Mode, the watchdog is disabled, and therefore no reset or interrupt is generated due to a watchdog failure.

Depending on the configuration, the **WD_FAIL** bits are set after a watchdog trigger failure as follows:

- If an incorrect watchdog trigger is received (triggering during the closed window or when the watchdog counter expires without a valid trigger), the **WD_FAIL** bits are incremented, indicating the number of incorrect triggers.
- For Configuration 2, the bits can reach a maximum value of '01'.
- For Configurations 1, 3, and 4, the bits can reach a maximum value of '10'.

The **WD_FAIL** bits are automatically cleared under the following conditions:

- After a successful watchdog trigger.
- When the watchdog is OFF, such as: in SBC Stop Mode after successful deactivation, in SBC Sleep Mode, or in SBC Fail-Safe Mode (except for a watchdog failure).

15.2.1 Time-Out Watchdog

The time-out watchdog is a simpler and less secure type of watchdog compared to the window watchdog, since the watchdog trigger can be performed at any time within the configured watchdog timer period.

A correct watchdog service immediately initiates a new watchdog timer cycle. Considering the tolerances of the internal oscillator, the safe trigger area is defined as shown in **Figure 53**.

If the time-out watchdog period expires, a watchdog reset is generated by pulling the reset output (RO) low, and the SBC transitions to SBC Restart Mode or SBC Fail-Safe Mode.

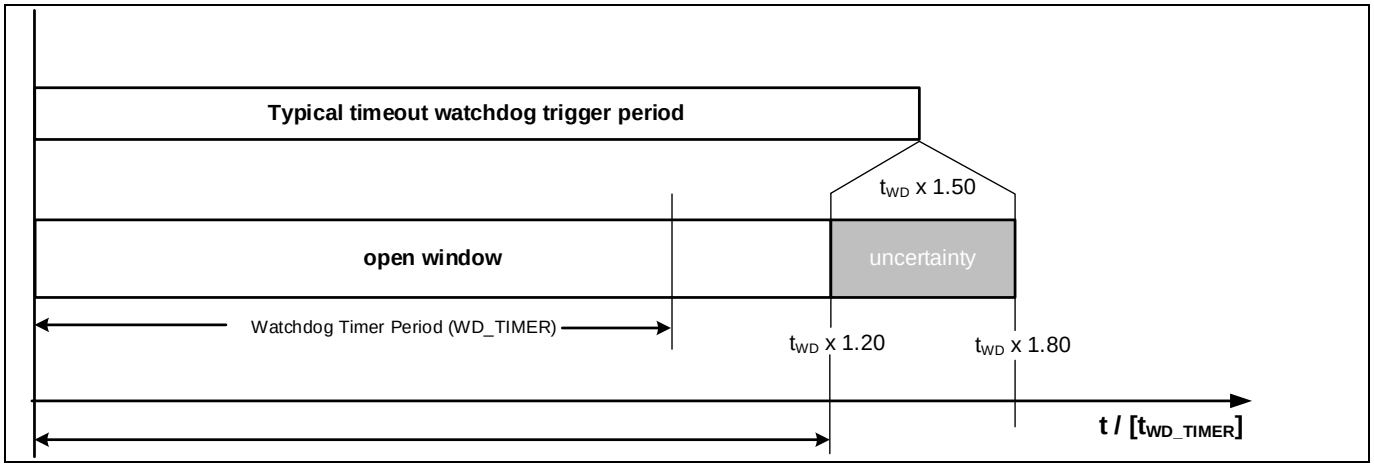


Figure 53 Time-out Watchdog Definition

15.2.2 Window Watchdog

Compared to the time-out watchdog, the window watchdog is characterized by dividing the watchdog timer period into a closed window and an open window. The watchdog must be triggered within the open window only.

A correct watchdog trigger initiates a new window watchdog period, starting with a closed window followed by an open window.

The watchdog timer period also represents the typical trigger time and defines the center of the open window. Considering the oscillator tolerances, the safe trigger area is defined as:

t_{WD} x 0.72 < safe trigger area < t_{WD} x 1.20.

The typical closed window has a width of 60 % of the selected window watchdog timer period. Taking the internal oscillator tolerances into account results in the timing relationships illustrated in **Figure 54**.

A correct watchdog service immediately starts the next closed window.

If the trigger signal occurs during the closed window, or if the watchdog timer period expires without a valid trigger, a watchdog reset is generated by pulling the reset output (RO) low, and the SBC transitions to SBC Restart Mode or SBC Fail-Safe Mode.

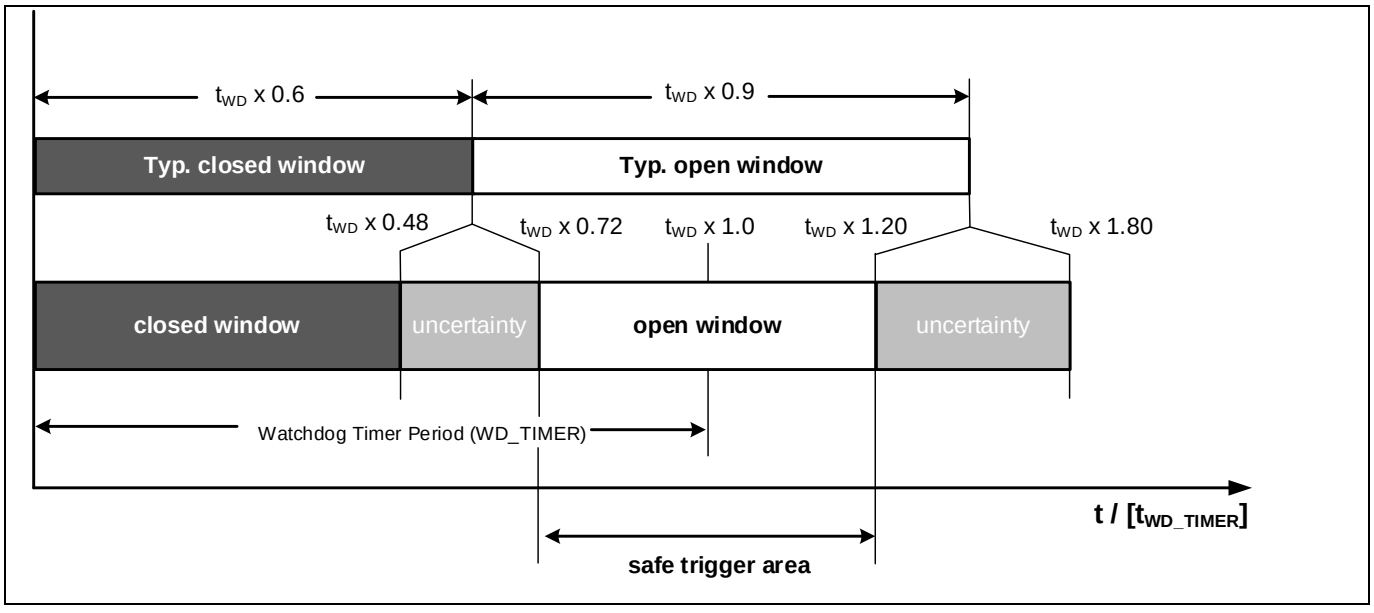


Figure 54 Window Watchdog Definition

15.2.3 Watchdog Setting Check Sum

A checksum bit is part of the SPI command used to trigger the watchdog and to set the watchdog configuration.

The sum of the eight data bits in the WWD_CTRL register must have even parity (refer to **Equation (15.1)**). This parity condition is achieved by appropriately setting the **CHECKSUM** bit to either '0' or '1'. If the checksum is incorrect, the SPI command is ignored—that is, the watchdog is not triggered, the settings are not updated, and the SPI_FAIL bit is set accordingly.

The checksum calculation includes all eight data bits of the WWD_CTRL register. The written value of the reserved bit 3 is also considered in this calculation, even if it is read as '0' in the SPI output. Therefore, if a '1' is written into the reserved bit 3 position, a '1' is used for the checksum computation.

$$CHKSUM = Bit15 \oplus \ldots \oplus Bit8 \quad (15.1)$$

15.2.4 Watchdog during SBC Stop Mode

The watchdog can be disabled for SBC Stop Mode while the device is operating in SBC Normal Mode. For safety reasons, a specific sequence must be followed to disable the watchdog, as illustrated in **Figure 55**. Two distinct SPI bits, **WD_STM_ EN_0** and **WD_STM_ EN_1**, located in the **WK_CTRL_1** and **WD_CTRL** registers respectively, must be set accordingly to complete the watchdog disable procedure.

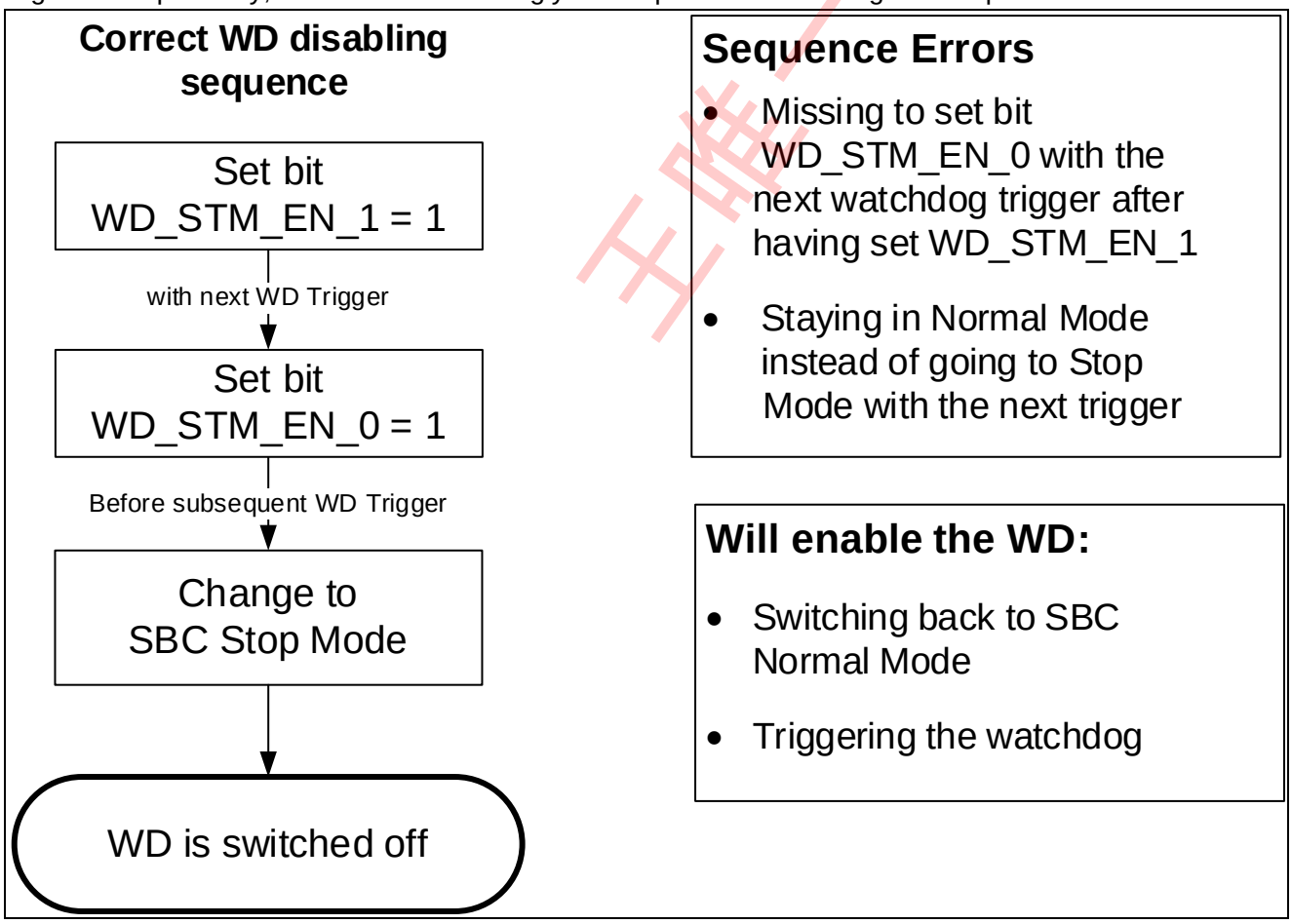


Figure 55 Watchdog disabling sequence in SBC Stop Mode

If a sequence error occurs, the bit **WD_STM_ EN_1** will be cleared, and the watchdog disable sequence must be restarted.

The watchdog can be re-enabled either by triggering the watchdog in SBC Stop Mode or by switching back to SBC Normal Mode via a SPI command. In both cases, the watchdog starts with a long open window, and the bits WD_STM_EN_1 and WD_STM_EN_0 are cleared. After the long open window, the watchdog must be served according to the configuration defined in the **WD_CTRL** register.

Note: The bit WD_STM_EN_0 is automatically cleared when the sequence is started, if it was previously set to 1.

15.2.5 Watchdog Start in SBC Stop Mode due to Bus Wake

In SBC Stop Mode, the watchdog can be disabled. Additionally, a BUS Wake feature is available that allows the watchdog to start automatically upon any BUS wake event (either CAN or LIN) during SBC Stop Mode. This feature is enabled by setting the bit **WD_EN_WK_BUS** = 1, which is the default value after Power-On Reset (POR). The bit can only be modified in SBC Normal Mode and must be programmed before initiating the watchdog disable sequence.

A wake-up event on the CAN or LINx bus generates an interrupt, and the respective RXD pin (for LINx or CAN) is pulled low. These signals inform the microcontroller that the watchdog has been started with a long open window. After this long open window, the watchdog must be served according to the configuration defined in the **WD_CTRL** register.

To disable the watchdog again, the SBC must be switched back to Normal Mode, and the disable sequence must be re-executed.

15.3 VS Power On Reset

At power-up of the device, the VS Power-On Reset is detected when VS > $V_{POR,r}$, and the SPI bit **POR** is set to indicate that all SPI registers are initialized to their POR default settings. During startup, VCC1 begins to rise, while the RESET output is held LOW. It will only be released once VCC1 has exceeded $V_{RT1,r}$ and the delay time t_{RD1} has elapsed.

If VS < $V_{POR,f}$, an internal device reset is generated, causing the SBC to be switched OFF. The device will then restart in INIT Mode at the next rising edge of VS. This behavior is illustrated in **Figure 56**.

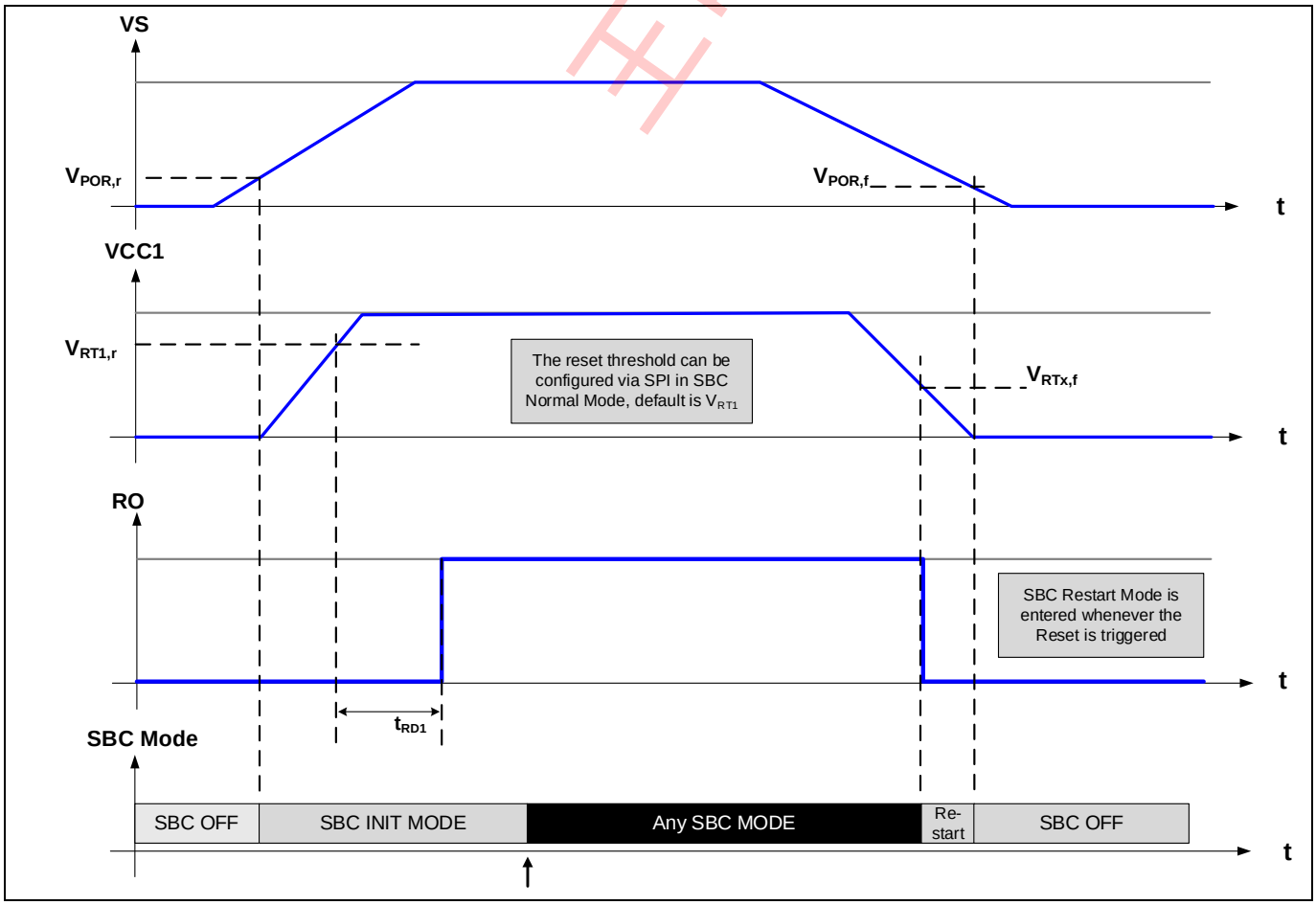


Figure 56 Ramp up / down example of Supply Voltage

15.4 Undervoltage VS and VSHS

When the supply voltage VS reaches the undervoltage threshold ($\mathbf{V_{S,UV}}$), the SBC performs the following actions:

- The SPI bit **VS_UV** is set. No other error bits are affected. The bit can be cleared once the condition is no longer present.
- VCC3 is disabled (refer to **Chapter 8.2**), unless the control bit **VCC3_VS_ UV_OFF** is set.
- The VCC1 short-circuit protection becomes inactive (refer to **Chapter 15.7**), while the thermal protection of the device remains active.

Once the undervoltage condition is recovered (i.e., VS rises above VS,UV), all functions are automatically re-enabled.

When the supply voltage VSHS drops below the undervoltage threshold ($\mathbf{V_{SHS,UVD}}$), the SBC executes the following measures:

- HS1 ... HS4 operate according to the SPI configuration (refer to **Chapter 9**).
- LINx: The transmitter and receiver are disabled during the VSHS undervoltage condition (refer to **Chapter 11.2.7**).
- The SPI bit **VSHS_UV** is set. No other error bits are affected. The bit can be cleared once the condition is no longer present.
- VCC1, VCC2, WKx, and CAN are not affected by the VSHS undervoltage.

15.5 Overvoltage VSHS

When the supply voltage VSHS reaches the overvoltage threshold ($\mathbf{V_{SHS,OVD}}$), the SBC triggers the following actions:

- HS1 ... HS4 operate according to the SPI configuration (refer to **Chapter 9**).
- The SPI bit **VSHS_OV** is set. No other error bits are affected. The bit can be cleared once the condition is no longer present.
- VCC1, VCC2, VCC3, WKx, LIN, and CAN are not affected by the VSHS overvoltage.

15.6 VCC1 Over-/ Undervoltage and Undervoltage Prewarning

15.6.1 VCC1 Undervoltage and Undervoltage Prewarning

A first-level voltage detection threshold is implemented as a prewarning for the microcontroller. The prewarning event is signaled with the bit **VCC1_ WARN**. No other actions are taken.

As described in **Chapter 15.1** and **Figure 57**, a reset will be triggered (RO pulled 'low') when the V_{CC1} output voltage falls below the selected undervoltage threshold (V_{RTx}). The bit **VCC1_UV** is set and the SBC will enter SBC Restart Mode.

Note: The **VCC1_WARN** or **VCC1_UV** bits are not set in Sleep Mode as V_{CC1} = 0V in this case

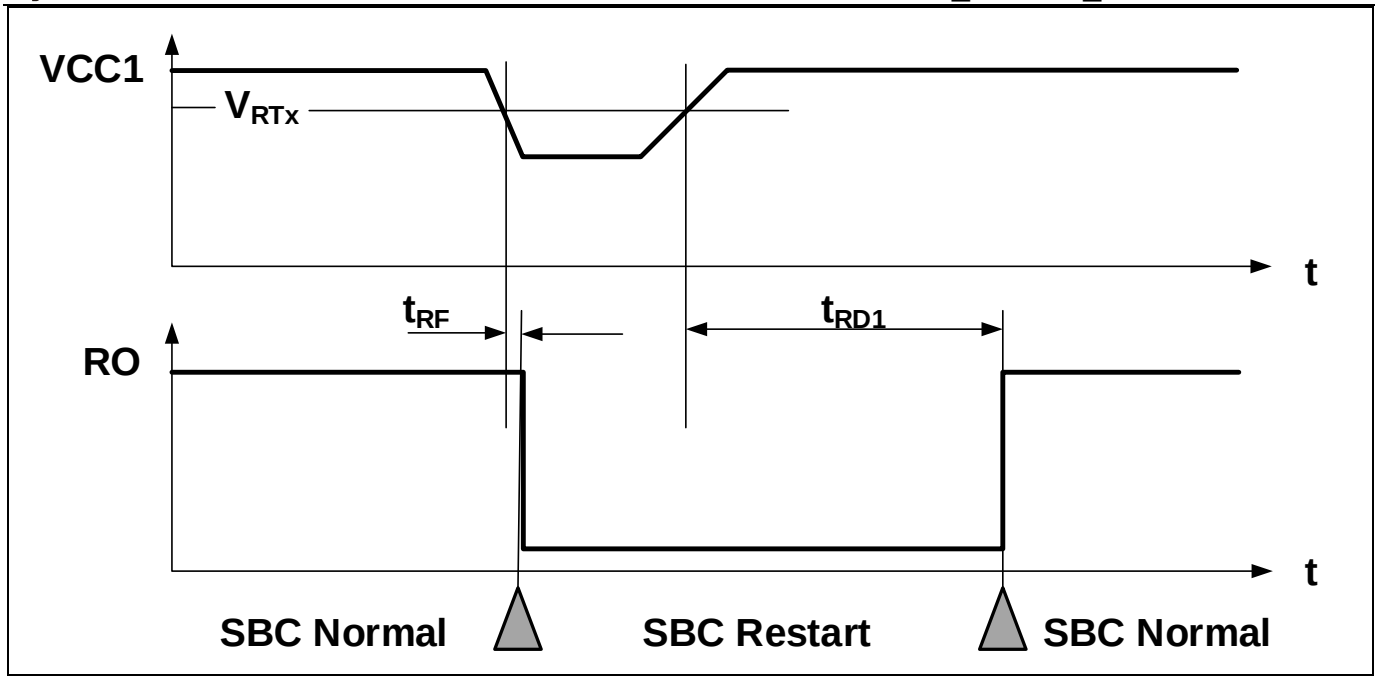


Figure 57 VCC1 Undervoltage Timing Diagram

An additional safety mechanism is implemented to prevent repetitive VCC1 undervoltage resets caused by high dynamic loads on VCC1. This mechanism operates through an internal event counter that monitors consecutive undervoltage occurrences.

- The counter is incremented for each consecutive VCC1 undervoltage event, regardless of the selected reset threshold.
- The counter remains active in SBC Init-, Normal-, and Stop Mode.
- When VS < V_{SUV} , the counter operation is stopped in SBC Normal Mode (the VS UV comparator remains enabled during this mode).
- Upon the 4th consecutive VCC1 undervoltage event, the SBC will enter Fail-Safe Mode, and the bit **VCC1_UV _FS** will be set.
- The counter is cleared under the following conditions:
  – when the SBC enters Fail-Safe Mode,
  – when the bit VCC1_UV is cleared,
  – or when a Soft Reset is triggered.

Note: It is recommended to clear the VCC1_UV bit once it has been set and detected to avoid unintended Fail-Safe transitions.

15.6.2 VCC1 Overvoltage

For fail-safe reasons, a configurable VCC1 overvoltage detection feature is implemented for both SBC Init Mode and SBC Normal Mode.

When the VCC1 output voltage exceeds the overvoltage threshold ($V_{CC1,OV,r}$), the SBC executes the following measures depending on the configuration:

- The status bit **VCC1_ OV** is always set.
- If the bit **VCC1_OV_RST** is set and **CFGP** = '1', the SBC will enter Restart Mode.
- The FOx outputs are activated, and after the reset delay time (t_{RD1}), the SBC Restart Mode is automatically left, resuming Normal Mode operation even if the VCC1 overvoltage condition persists (refer to **Figure 58**). The **VCC1_OV_RST** bit is cleared automatically after this sequence.
- If the bit **VCC1_OV_RST** is set and **CFGP** = '0', the SBC will enter Fail-Safe Mode, and the FOx outputs are activated accordingly.

Note: Before entering SBC Stop Mode the bit **VCC1_OV_RST** must be set to '0' to avoid unintentional SBC Restart or Fail-Safe Mode entry. The status bit **VCC1_OV** could be set unintentionally. The reason is that external noise could be coupled into the VCC1 supply line. Especially, in case the VCC1 output current in SBC STOP Mode is below the active peak threshold ($I_{VCC1,Ipeak}$).

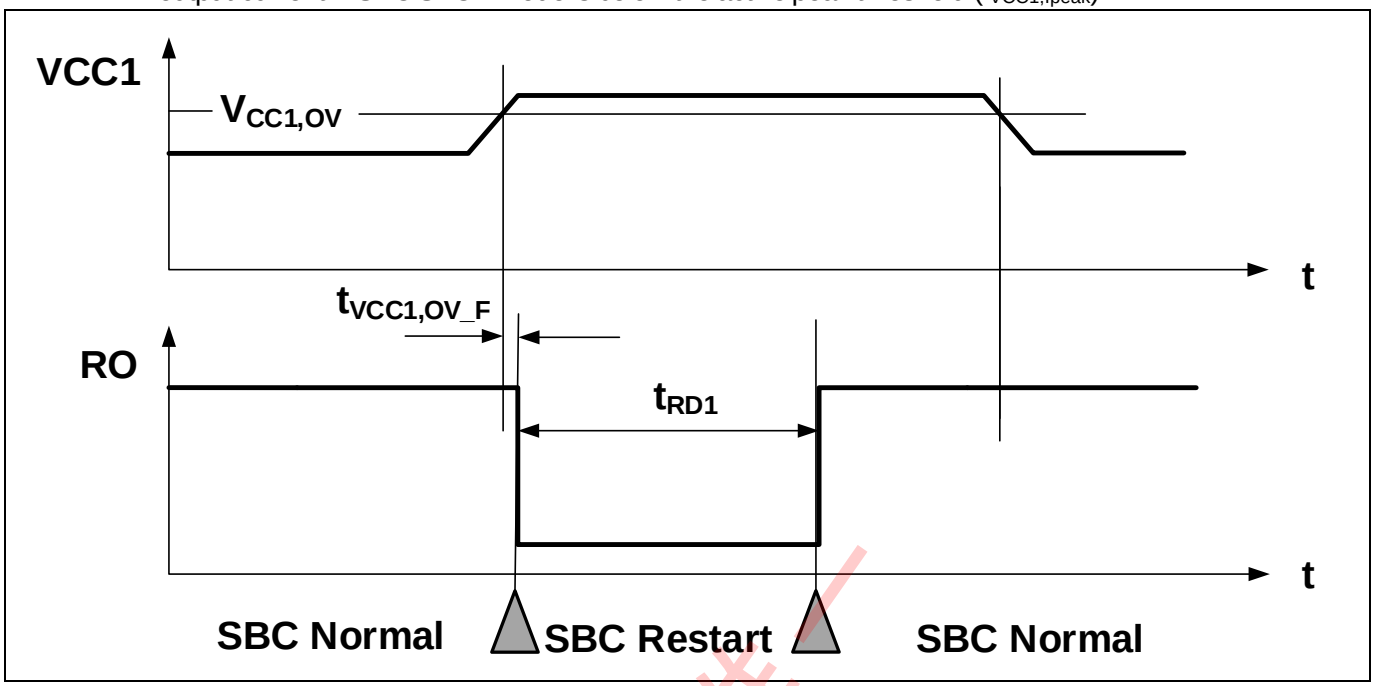


Figure 58 VCC1 Overvoltage Timing Diagram

15.7 VCC1 Short Circuit and VCC3 Diagnostics

The short-circuit protection for VCC1 is implemented under the condition that VS > $V_{S,UV}$. The protection operates as follows:

- If VCC1 does not exceed the threshold VRTx within $t_{VCC1,SC}$ after device power-up or wake-up from SBC Sleep Mode, the SPI bit **VCC1_SC** is set, VCC1 is turned OFF, the FOx pins are enabled, the FAILURE flag is set, and the SBC enters Fail-Safe Mode. The SBC can be reactivated via wake-on CAN, LINx, or WKx.
- The same reaction occurs if VCC1 falls below VRTx for a duration longer than $t_{VCC1,SC}$.

The VCC3 diagnostic functions operate differently depending on configuration:

- Load-Sharing : The external PNP transistor is disabled when VS <$V_{S,UV}$ if VCC3_VS_UV_OFF = '0', or when in SBC Stop Mode if **VCC3_LS_STP_ON** = '0'. All other diagnostic features are disabled, as they are provided through VCC1.
- Stand-Alone Configuration: The external PNP transistor is disabled when VS < $V_{S,UV}$ if VCC3_VS_UV_OFF = '0'. Overcurrent limitation is indicated by the bit **VCC3_OC** , depending on the selected shunt resistor. Undervoltage/Overvoltage conditions are signaled via bits **VCC3_UV/VCC3_OV** respectively. The regulator is disabled when VS undervoltage threshold is reached.

Note: Neither **VCC1_SC** nor **VCC3_UV**/VCC3_OV flags are set during power-up of V_{CC1} or activation of V_{CC3}, respectively.

15.8 VCC2 Under-/Over-voltage and VCAN Undervoltage

Under-voltage and over-voltage warning mechanisms are implemented for VCC2 and VCAN as described below:

- V_{CC2} Under-/Over-Voltage Detection: When V_{CC2} drops below the under-voltage threshold ($V_{CC2,UV,f}$), the SPI bit **VCC2_UV** is set and can be cleared only via SPI. When V_{CC2} rises above the over-voltage threshold ($V_{CC2,OV,r}$), the SPI bit **VCC2_OV** is set and can be cleared only via SPI.
- V_{CAN} Undervoltage Detection: When the V_{CAN} voltage drops below the undervoltage threshold ($V_{CAN,UV}$), the SPI bit **VCAN_UV** is set and can be cleared only via SPI.

Note: The VCC2_UV/VCC2_OV flag is not set during turn-on or turn-off of V_{CC2}.

15.9 Thermal Protection

Three independent thermal protection mechanisms are implemented in the SBC to safeguard against temperature-related faults, each addressing a different level of system impact:

- Individual thermal shutdown of specific blocks
- Temperature prewarning of main microcontroller supply VCC1
- SBC thermal shutdown due to VCC1 overtemperature

15.9.1 Individual Thermal Shutdown

As a first-level protection measure, the output stages VCC2, VCC3, CAN, LINx, and HSx are independently switched OFF when the respective block reaches the junction temperature threshold (T_{jTSD1}). Once this condition is detected, the **TSD1** bit is set. This bit can be cleared only via SPI after the overtemperature condition is no longer present. The thermal shutdown protection is active only when the respective block is ON, regardless of the current SBC Mode.

The respective modules behave as follows:

- VCC2: When VCC2 reaches the T_{jTSD1} threshold, it is switched OFF, and the control bits **VCC2_ON** are cleared. The status bit **VCC2_OT** is set. After the temperature returns below the threshold, VCC2 must be re-configured via SPI.
- VCC3 (Stand-Alone Regulator): The regulator is switched OFF, and the control bits **VCC3_ON** are cleared. The status bit **VCC3_OT** is set. Once the temperature normalizes, VCC3 must be re-configured via SPI. It is recommended to clear **VCC3_OT** before re-enabling the regulator.
- VCC3 (Load-Sharing Configuration): In case of overtemperature, the bit **VCC3_OT** is set, and VCC3 is switched OFF. The regulator is automatically re-enabled once the overtemperature condition disappears. It is also recommended to clear VCC3_OT immediately after recovery.
- CAN Transceiver: The CAN transmitter is disabled and remains in CAN Normal Mode, functioning as Receive-Only Mode. The status bits **CAN_FAIL** = '01' are set. Once the temperature returns to normal, the CAN transmitter is automatically re-enabled.
- LINx Transceiver: The LIN transmitter is disabled and stays in LIN Normal Mode, operating as Receive-Only Mode. The status bits **LIN2_FAIL** = '01' are set. When the temperature is back within limits, the LIN transmitter is automatically re-enabled.
- HSx Switches: If one or more HSx switches reach the T_{jTSD1} threshold, all HSx switches are turned OFF, and their control bits are cleared (see registers **HS_CTRL1** and **HS_CTRL2**). The status bits HSx_OC_OT are set (see register **HS_OC_OT_STAT**). After recovery, the HSx configuration must be restored via SPI.

Note: The diagnosis bits are not cleared automatically and have to be cleared via SPI once the overtemperature condition is not present anymore.

15.9.2 Temperature Prewarning

As the second-level thermal protection, a temperature prewarning mechanism is implemented when the main supply VCC1 reaches the thermal prewarning threshold (T_{jPW}). Once this threshold is reached, the status bit **TPW** is set. This bit can be cleared only via SPI after the overtemperature condition is no longer present. The temperature prewarning function is active only when VCC1 is ON, regardless of the current SBC Mode.

15.9.3 SBC Thermal Shutdown

As the highest-level thermal protection, an SBC-level thermal shutdown is triggered when the main supply VCC1 reaches the thermal shutdown threshold (T_{jTSD2}). Upon detection of a TSD2 event, the SBC

enters Fail-Safe Mode for a duration of t_{TSD2}, allowing the device to cool down. After this period expires, the SBC automatically transitions through Restart Mode to Normal Mode (refer to **Chapter 5.1.6**).

When a TSD2 event occurs, the status bit **TSD2** is set. This bit can be cleared only via SPI in SBC Normal Mode, once the overtemperature condition has been resolved. Similar to the prewarning mechanism, the thermal shutdown is active only when VCC1 is ON, independent of the SBC Mode.

15.10 Electrical Characteristics

Table 35 Electrical Specification

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			
VCC1 Monitoring							
Undervoltage Prewarning Threshold Voltage PW,f	$V_{PW,f}$(5V)	4.6	4.7	4.85	V	VCC1 falling, SPI bit is set	
	$V_{PW,f}$(3V3)	3.0	3.1	3.2			
Undervoltage Prewarning Threshold Voltage PW,r	$V_{PW,r}$(5V)	4.65	4.80	4.90	V	VCC1 rising	
	$V_{PW,r}$(3V3)	3.1	3.2	3.28			
Reset Threshold Voltage RT1,f	$V_{RT1,f}$(5V)	4.5	4.6	4.75	V	default setting; VCC1 falling	
	$V_{RT1,f}$(3V3)	2.95	3.05	3.15			
Reset Threshold Voltage RT1,r	$V_{RT1,r}$(5V)	4.6	4.7	4.85	V	default setting; VCC1 rising	
	$V_{RT1,r}$(3V3)	3.0	3.1	3.2			
Reset Threshold Voltage RT2,f	$V_{RT2,f}$(5V)	3.75	3.9	4.05	V	VCC1 falling	
	$V_{RT2,f}$(3V3)	2.5	2.6	2.7			
Reset Threshold Voltage RT2,r	$V_{RT2,r}$(5V)	3.85	4.0	4.15	V	VCC1 rising	
	$V_{RT2,r}$(3V3)	2.55	2.65	2.75			
Reset Threshold Voltage RT3,f	$V_{RT3,f}$(5V)	3.15	3.3	3.45	V	VS ≥ 4V; VCC1 falling	
	$V_{RT3,f}$(3V3)	2.2	2.3	2.4			
Reset Threshold Voltage RT3,r	$V_{RT3,r}$(5V)	3.25	3.4	3.55	V	VS ≥ 4V; VCC1 rising	
	$V_{RT3,r}$(3V3)	2.25	2.35	2.45			
Reset Threshold Voltage RT4,f	$V_{RT4,f}$(5V)	2.4	2.65	2.8	V	VS ≥ 4V; VCC1 falling	
	$V_{RT4,f}$(3V3)	2.0	2.1	2.2			
Reset Threshold Voltage RT4,r	$V_{RT4,r}$(5V)	2.5	2.75	2.9	V	VS ≥ 4V; VCC1 rising	
	$V_{RT4,r}$(3V3)	2.05	2.15	2.25			
Reset Threshold Hysteresis	$V_{RT,hys}$(5V)	50	100	200	mV	–	
	$V_{RT,hys}$(3V3)	30	67	140			
VCC1 Overvoltage Detection Threshold Voltage	$V_{CC1,OV,r}$(5V)	5.3	–	5.6	V	[1)]rising VCC1	
	$V_{CC1,OV,r}$(3V3)						
VCC1 Overvoltage Detection Threshold Voltage	$V_{CC1,OV,f}$(5V)	5.2	–	5.5	V	falling VCC1	
	$V_{CC1,OV,f}$(3V3)						
VCC1 OV Detection Filter Time	t_{VCC1,OV_F}	5	10	14	us	[3)]	
VCC1 Short to GND Filter Time	$t_{VCC1,SC}$	3.2	4	4.8	ms	[3)]	
Reset Generator; Pin RO							
Reset Low Output Voltage	$V_{RO,L}$	–	0.2	0.4	V	I_{RO} = 1 mA for	

						$V_{CC1} \geq 1\,V$ & $V_S \geq V_{POR,f}$	
Reset High Output Voltage	$V_{RO,H}$	0.8 x V_{CC1}	–	V_{CC1} + 0.3 V	V	I_{RO} = -20 µA	

Table 35 Electrical Specification (cont'd)

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			
Reset Pull-up Resistor	R_{RO}	10	20	40	kΩ	V_{RO} = 0 V	
Reset Filter Time	t_{RF}	4	10	26	µs	[3]$V_{CC1} < V_{RT1x}$ to RO = L see also **Chapter 15.3**	
Reset Delay Time	t_{RD1}	1.5	2	2.5	ms	2) 3)	
VCC2 Monitoring							
VCC2 Undervoltage Threshold Voltage (falling)	$V_{CC2,UV,f}$	4.5	–	4.75	V	VCC2 falling	
VCC2 Undervoltage Threshold Voltage (rising)	$V_{CC2,UV,r}$	4.6	–	4.9	V	VCC2 rising	
VCC2 Undervoltage detection hysteresis	$V_{CC2,UV,hys}$	20	100	250	mV	–	
VCC2 Overvoltage Detection Threshold Voltage	$V_{CC2,OV,r}$	5.3	–	5.5	V	VCC2 rising	
VCC2 Overvoltage Detection Threshold Voltage	$V_{CC1,OV,f}$	5.2	–	5.4	V	VCC2 falling	
VCC3 Monitoring							
VCC3 Undervoltage Detection	$V_{CC3,UV}$	4.0	4.25	4.5	V	5V setting	
VCC3 Undervoltage Detection	$V_{CC3,UV}$	2.65	2.85	3.00	V	3.3V setting	
VCC3 Undervoltage Detection	$V_{CC3,UV}$	1.4	1.52	1.65	V	1.8V setting	
VCC3 Undervoltage Detection	$V_{CC3,UV,hys}$	20	100	250	mV		
VCC3 Overvoltage Detection	$V_{CC3,OV}$	5.3	5.55	5.8	V	5V setting	
VCC3 Overvoltage Detection	$V_{CC3,OV}$	3.5	3.65	3.85	V	3.3V setting	
VCC3 Overvoltage Detection	$V_{CC3,OV}$	1.95	2.08	2.2	V	1.8V setting	
VCC3 Overvoltage Detection	$V_{CC3,OV,hys}$	20	100	250	mV		
VCAN Monitoring							

CAN Supply undervoltage detection threshold	V_{CAN_UV}	4.45	–	4.85	V	CAN Normal Mode, hysteresis included;	
Watchdog Generator							
Long Open Window	t_{LW}	160	200	240	ms	3)4)	
Internal Oscillator	f_{CLKSBC}	0.8	1.0	1.2	MHz	–	
Minimum Waiting time during SBC Fail-Safe Mode							
Min. waiting time Fail-Safe	$t_{FS,min}$	80	100	120	ms	3)5)	
Power-on Reset, Over- / Undervoltage Protection							
VS Power on reset rising	$V_{POR,r}$	–		5.0	V	VS increasing	
VS Power on reset falling	$V_{POR,f}$	–		3.2	V	VS decreasing	

Table 35 Electrical Specification (cont'd)

V_S = 5.5 V to 28 V; T_j = -40 °C to +150 °C; SBC Normal Mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			
VS Undervoltage Detection Threshold	$V_{S,UV}$	5.3	–	6.0	V	Supply UV threshold for VCC3 and VCC1 SC detection; hysteresis included	
VSHS Overvoltage Detection Threshold	$V_{SHS,OVD}$	20		22	V	Supply OV supervision for HSx; hysteresis included	
VSHS Overvoltage Detection hysteresis	$V_{SHS,OVD,hys}$	100	500	–	mV	6)	
VSHS Undervoltage Detection Threshold	$V_{SHS,UVD}$	4.8		5.5	V	Supply UV supervision for LINx, HSx, and HS of GPIOx; hysteresis included	
VSHS Undervoltage Detection hysteresis	$V_{SHS,UVD,hys}$	50	200	350	mV	6)	
Overtemperature Shutdown[6)]							
Thermal Prewarning Temperature	T_{jPW}	135	145	155	°C		
Thermal Shutdown TSD1	T_{jTSD1}		165		°C	7)	
Thermal Shutdown TSD2	T_{jTSD2}		165		°C	7)	

Thermal Shutdown hysteresis	$T_{jTSD,hys}$		25		°C	7)	
Deactivation time after thermal shutdown TSD2	t_{TSD2}	0.8	1	1.2	s	3)	

1) It is ensured that the threshold $V_{CC1,OV,r}$ is always higher than the highest regulated V_{CC1} output voltage $V_{CC1,out42}$.
2) The reset delay time will start when VCC1 crosses above the selected Vrtx threshold
3) Not subject to production test, tolerance defined by internal oscillator tolerance.
4) An additional safety factor of 1.5 needs to be applied like shown in **Figure 53**.
5) This time applies for all failure entries except a device thermal shutdown (TSD2 has a typ. 1s waiting time t_{TSD2})
6) Not subject to production test, specified by design.
7) Subject to change according to the final implementation.

16 Serial Peripheral Interface

16.1 SPI Block Description

The 16-bit Control Input Word is received through the data input pin SDI, synchronized with the clock signal CLK generated by the microcontroller. The corresponding output word is transmitted simultaneously on the SDO line (see **Figure 59**).

Communication starts when the device is activated by pulling the CSN (Chip Select Not) input low. Once CSN returns high, the received word is processed according to its content. At this moment, the SDO output enters a high-impedance (tristate) condition, freeing the bus for other devices.

During operation, the SDI data is loaded into the input register on each falling edge of CLK, while the SDO data is shifted out from the output register on each rising edge. The SBC's SPI interface does not support daisy-chain configurations.

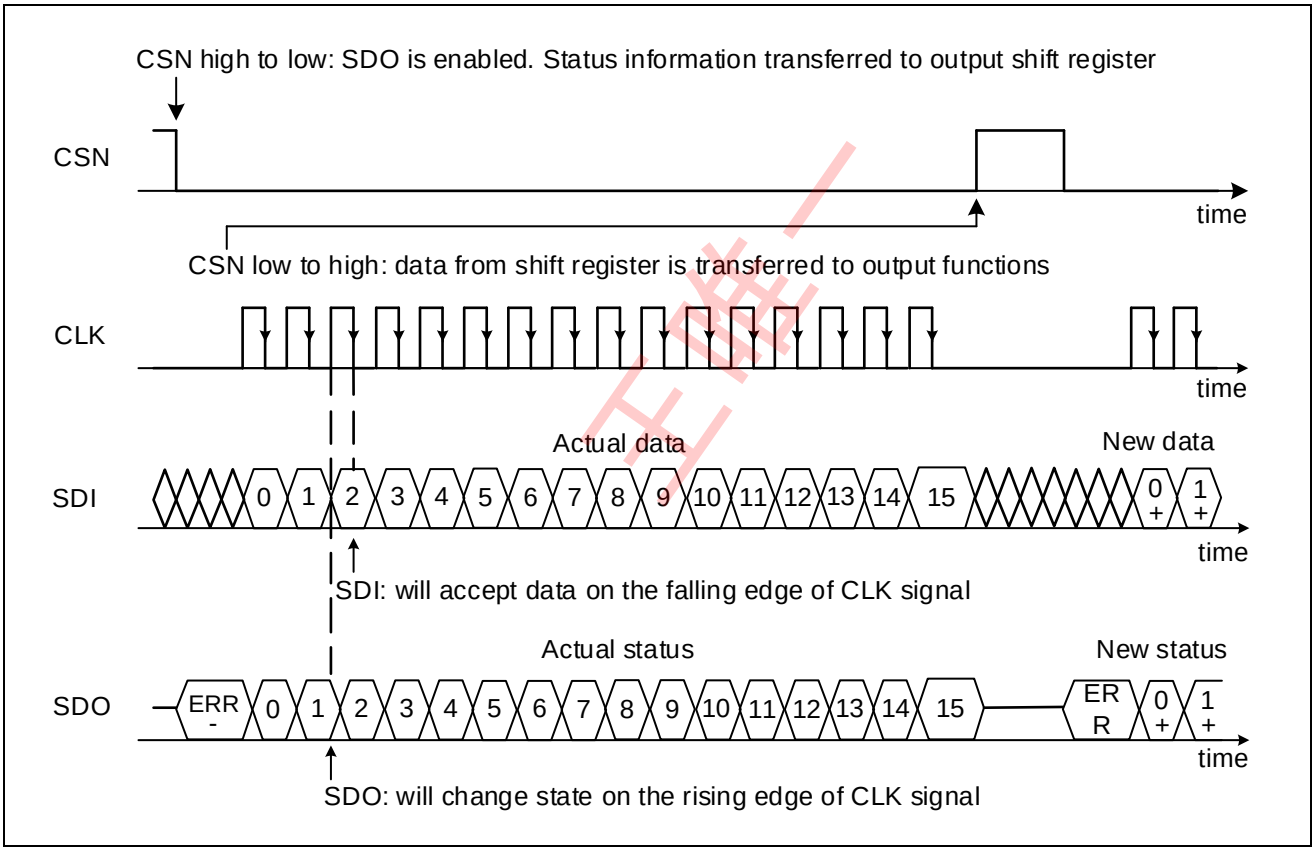


Figure 59 SPI Data Transfer Timing (note the reversed order of LSB and MSB shown in this figure compared to the register description)

16.2 Failure Indication on SPI Data Output

If the microcontroller issues an incorrect SPI command to the SBC, the SBC disregards the received data. Invalid commands include unsupported mode selections or instructions blocked by the internal state machine to prevent unintended device or system behavior (see below). In such cases, the diagnostic flag 'SPI_FAIL' is set, and the SPI Write operation is ignored—typically without any partial execution. This flag can only be cleared explicitly through a dedicated SPI command.

nvalid SPI Commands Leading to SPI_FAIL:

- Illegal state transitions: Attempting to switch directly from SBC Stop to SBC Sleep Mode will force the SBC into Restart Mode.
  Trying to enter SBC Stop or SBC Sleep Mode from SBC Init Mode results in a transition to Normal Mode instead;
- Parity error in **WD_CTRL** register: If the data bit parity in WD_CTRL is invalid, the watchdog trigger or updated watchdog configuration will be ignored;
- SPI access in Stop Mode: Any attempt to modify SPI settings such as watchdog, PWM, or high-side configuration while in SBC Stop Mode is ignored;
- Only the following commands are accepted in this mode: watchdog trigger, return to Normal Mode, initiate Soft Reset, and read & clear status registers;
- Entering Stop Mode with uncleared wake flags: If **WK_STAT_1** and **WK_STAT_2** are not cleared before entering Stop Mode, **SPI_FAIL** will not be set, but the INT pin will be activated.
- Transition from Stop to Normal Mode: When switching from Stop to Normal Mode, any additional modifications to the **M_S_CTRL** register are ignored;
- Invalid Sleep Mode entry: Attempting to enter Sleep Mode while all bits in **BUS_CTRL_1**, **BUS_CTRL_2**, and **WK_CTRL_2** are cleared triggers **SPI_FAIL**, and the SBC enters Restart Mode. Although Sleep Mode is not entered, other parts of the command (e.g., changes to VCC2 or VCC3) are executed, and their values remain unchanged during Restart Mode. Note: At least one wake source must be enabled to avoid a deadlock in Sleep Mode. If the only wake source is a timer and it is turned off, the SBC will immediately exit Sleep Mode and enter Restart Mode. No failure handling occurs when entering Stop Mode with all bits in **BUS_CTRL_1**, **BUS_CTRL_2** and **WK_CTRL_2** cleared, since the microcontroller can still exit this mode via SPI.
- VCC3 load sharing: If **VCC3_LS** (load sharing) is active and the microcontroller attempts to clear this bit, the rest of the command is executed, but **VCC3_LS** remains set.
- Invalid wake configuration for Sleep Mode: If WK_MEAS is set to '1' while only WK1_EN or WK2_EN are enabled as wake sources, the **SPI_FAIL** bit is set and the SBC enters Restart Mode.
- Timer configuration error: Setting an on-time equal to or longer than the corresponding timer period will trigger SPI_FAIL.
- SDI line stuck: If the SDI input remains constantly HIGH or LOW (receiving all '0's or all '1's), the SPI_FAIL condition is set.
- Note: There is no SPI fail information for unused addresses.

SPI Error Detection and ERR Flag Behavior:

The ERR flag provides an additional diagnostic mechanism for monitoring the integrity of SPI communication between the microcontroller and the SBC.

The flag is set under the following conditions:

- The number of received SPI clock pulses is not equal to 0 or 16.
- The RO pin is LOW while SPI frames are being transmitted.

Note: To ensure correct reading of the ERR flag, the CLK signal must be LOW when CSN is asserted. The ERR bit is invalid if CLK is HIGH during the falling edge of CSN.

Invalid Number of SPI Clock Cycles:

The SBC continuously monitors the number of SPI clock cycles received. Only 0 or 16 clock cycles are considered valid.

- If the number of received clocks differs from 0 or 16, the input word is discarded.
- A 0-clock condition is used to enable ERR signalization.
- The error logic additionally monitors whether CLK remains HIGH during CSN transitions.

If either of these conditions is detected—clock count mismatch or CLK HIGH during CSN edge—the SBC indicates an error by driving the ERR bit (SDO pin) HIGH before the first rising edge of the next SPI clock.

In this case, the entire SPI command is ignored.

SPI Frames Sent While RO is LOW:

When the RO pin is LOW (indicating the SBC is in Restart Mode), and SPI frames are transmitted simultaneously, the ERR flag will be set.

The error condition will be reported in the next SPI transaction under the following circumstances:

- if the command begins when RO is HIGH and it ends when RO is LOW,
- if a SPI command will be sent while RO is LOW,
- If a SPI command begins when RO is LOW and it ends when RO is HIGH.

SDO Output Behavior:

- always when RO is LOW then SDO will be HIGH,
- when a SPI command begins with RO is LOW and ends when RO is HIGH, then the SDO should be ignored because wrong data will be sent.

Notes

1. It is possible to quickly check for the ERR flag without sending any data bits.i.e. only the CSN is pulled low and SDO is observed- no SPI Clocks are sent in this case
2. The ERR flag could also be set after the SBC has entered SBC Fail-Safe Mode because the SPI communication is stopped immediately.

16.3 SPI Programming

For the GD33AP236x, seven bits (BIT6...0) are used for address selection. Bit 7 defines the access type: for status registers it selects between Read Only and Read & Clear, and for configuration registers it selects between Write and Read Only. The actual configuration and status information is contained in eight data bits (BIT15...8). All write, clear, and read operations are executed byte-wise. The SPI status bits are not cleared automatically and must be cleared by the microcontroller, for example, if the TSD2 bit was set due to an overtemperature condition. Configuration bits may be partially cleared automatically by the SBC; detailed behavior is described in the individual register descriptions. During SBC Restart Mode, SPI communication is ignored by the SBC and incoming SPI frames are not interpreted.

There are two types of SPI registers: control registers, which configure the SBC (e.g., SBC mode, watchdog trigger), and status registers, which indicate the SBC status (e.g., wake events, warnings, failures). For status registers, the requested information is returned in the same SPI command via the DO line. For control registers, the status of the respective byte is also shown in the same SPI command; however, if a setting is changed, the updated value is valid only after CSN returns high and is shown with the next SPI command to the same register.

The SBC status information from the SPI status registers is transmitted in a compressed format with each SPI response on the SDO line, within the so-called Status Information Field register. The purpose of this register is to provide the microcontroller with a fast indication whenever a change occurs in any of the SPI status registers. This mechanism allows the microcontroller to avoid continuously reading all SPI status registers and instead read only those registers that have changed. Each bit in the Status Information Field corresponds to one SPI status register. When a bit in any of the status registers is set, the corresponding bit in the Status Information Field register is also set. The register **WK_LVL_STAT** is not included in the Status Information Field. For example, if bit 0 in the Status Information Field is set to 1, it indicates that one or more bits in the register with address 1000001 (**SUP_STAT_1**) are set to 1, and this register should then be read in a

subsequent SPI command. The respective bit in the Status Information Field will return to 0 once all bits in the corresponding status register 1000001 are cleared.

Table 36 Status Information Field

Bit in Status Information Field	Corresponding Address Bit	Status Register Description
0	100 0001	SUP_STAT_1: Supply Status - VSHS fail, VCCx fail, POR
1	100 0010	THERM_STAT: Thermal Protection Status
2	100 0011	DEV_STAT: Device Status - Mode before Wake, WD Fail, SPI Fail, Failure, Reference fail
3	100 0100	BUS_STAT: Bus Failure Status: CAN, LINx; BUS_STAT_1 & BUS_STAT_2 are a combinational OR
4	100 0110	WK_STAT_1,WK_STAT_2: Wake Source Status; Status bit is set as combinational OR of both registers
5	100 0000	SUP_STAT_2: VCC1_WARN/OV,VCC3 Status
6	101 0100	HS_OC_OT_STAT: High-Side Over Load Status
7	101 0101	HS_OL_STAT: High-Side Open Load Status

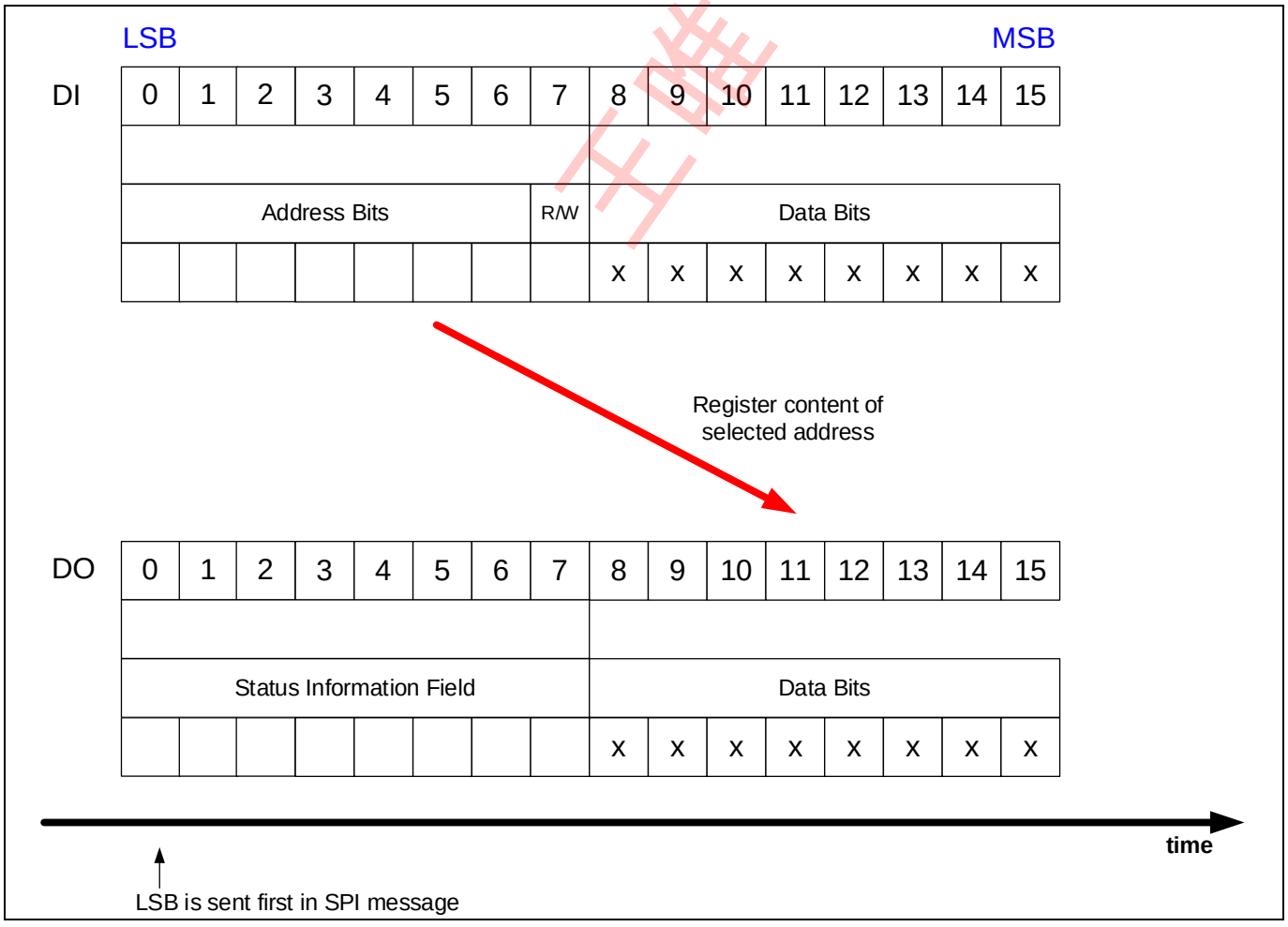


Figure 60 SPI Operation Mode

16.4 SPI Bit Mapping

The following figures illustrate the mapping of the registers and the corresponding SPI bits of each register. The control registers, ranging from addresses ‘0000000’ to ‘0011110’, are Read/Write registers. The

access type is defined by bit 7: when bit 7 is set to '0', the register is read only; when bit 7 is set to '1', the register is written. The updated bit settings after a write operation can be verified with the next read or write command. The registers from '1000000' to '1111110' are Status Registers and can either be read or read with clearing, depending on bit 7. To clear a data byte in one of the status registers, bit 7 must be set to '1'. Certain registers, including **WK_LVL_STAT**, and **FAM_PROD_STAT**, **SWK_OSC_CAL_H_STAT**, **SWK_OSC_CAL_L_STAT**, **SWK_STAT**, **SWK_ECNT_STAT**, **SWK_CDR_STAT1**, **SWK_CDR_STAT2**, are exceptions because they represent actual voltage levels at the respective wake pins (LOW/HIGH) or fixed family and product identification values, and therefore cannot be cleared. For reliable diagnostics, it is recommended to clear the relevant status bits associated with wake events or failures. However, in general, it is still possible to enable drivers without clearing the corresponding failure flags.

When switching to a different SBC mode, certain configuration bits are automatically cleared or modified according to the new operating state:

- The SBC mode bits are updated to reflect the actual status, for example, when returning to Normal Mode.
- When transitioning to a low-power mode such as Stop or Sleep, the diagnostic bits of the switches and transceivers are not cleared, and FOx remains active if it was previously triggered. In SBC Stop Mode, the CAN and LIN control bits remain unchanged.
- In SBC Sleep Mode, the CAN and LIN control bits are modified if they were not previously set to OFF or wake-capable.
- HSx, VCC2, and VCC3 remain active when entering Sleep or Stop Mode; their configuration can only be adjusted in Normal Mode. Diagnosis functions (OC, OL, OT) remain active, and in case of a failure, the corresponding switch is turned off without generating a wake-up signal.
- The configuration bits for HSx and VCC2 in stand-alone configuration are cleared during SBC Restart Mode, while FOx remains active if previously triggered. Depending on the configuration, CAN and LIN transceivers may be turned off, awakened, or remain wake-capable.
- The detailed behavior of the corresponding SPI bits and control functions is specified in Chapter 16.5, Chapter 16.6, and in the respective module chapters. Bits that can be modified by the SBC itself are marked as "rwh."

Note: The bit type be marked as 'rwh' in case the SBC will modify respective control bits. The detailed behavior of the corresponding SPI bits and control functions is specified in **Chapter 16.5**, **Chapter 16.6**, and in the respective module chapters. Bits that can be modified by the SBC itself are marked as "rwh.

	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0		
	8 Data Bits [bits 8... 15] for Configuration & Status Information								**Reg-Type**	**7 Address Bits [bits 0... 6]** for Register Selection								
Control Registers	M_S_CTRL								rw	0	0	0	0	0	0	1		
	HW_CTRL								rw	0	0	0	0	0	1	0		
	WD_CTRL								rw	0	0	0	0	0	1	1		
	BUS_CTRL_1								rw	0	0	0	0	1	0	0		
	BUS_CTRL_2								rw	0	0	0	0	1	0	1		
	WK_CTRL_1								rw	0	0	0	0	1	1	0		
	WK_CTRL_2								rw	0	0	0	0	1	1	1		
	WK_PUPD_CTRL								rw	0	0	0	1	0	0	0		
	WK_FLT_CTRL								rw	0	0	0	1	0	0	1		
	TIMER1_CTRL								rw	0	0	0	1	1	0	0		
	TIMER2_CTRL								rw	0	0	0	1	1	0	1		
	SW_SD_CTRL								rw	0	0	1	0	0	0	0		
	HS_CTRL_1								rw	0	0	1	0	1	0	0		
	HS_CTRL_2								rw	0	0	1	0	1	0	1		
	GPIO_CTRL								rw	0	0	1	0	1	1	1		
	PWM1_CTRL								rw	0	0	1	1	0	0	0		
	PWM2_CTRL								rw	0	0	1	1	0	0	1		
	PWM_FREQ_CTRL								rw	0	0	1	1	1	0	0		
	SYS_STAT_CTRL								rw	0	0	1	1	1	1	0		
Selective Wake Control Registers	SWK_CTRL								rw	0	1	0	0	0	0	0		
	SWK_BTL1_CTRL								rw	0	1	0	0	0	0	1		
	SWK_BTL2_CTRL								rw	0	1	0	0	0	1	0		
	SWK_ID3_CTRL								rw	0	1	0	0	0	1	1		
	SWK_ID2_CTRL								rw	0	1	0	0	1	0	0		
	SWK_ID1_CTRL								rw	0	1	0	0	1	0	1		
	SWK_ID0_CTRL								rw	0	1	0	0	1	1	0		
	SWK_MASK_ID3_CTRL								rw	0	1	0	0	1	1	1		
	SWK_MASK_ID2_CTRL								rw	0	1	0	1	0	0	0		
	SWK_MASK_ID1_CTRL								rw	0	1	0	1	0	0	1		
	SWK_MASK_ID0_CTRL								rw	0	1	0	1	0	1	0		
	SWK_DLC_CTRL								rw	0	1	0	1	0	1	1		
	SWK_DATA7_CTRL								rw	0	1	0	1	1	0	0		
	SWK_DATA6_CTRL								rw	0	1	0	1	1	0	1		
	SWK_DATA5_CTRL								rw	0	1	0	1	1	1	0		
	SWK_DATA4_CTRL								rw	0	1	0	1	1	1	1		
	SWK_DATA3_CTRL								rw	0	1	1	0	0	0	0		
	SWK_DATA2_CTRL								rw	0	1	1	0	0	0	1		
	SWK_DATA1_CTRL								rw	0	1	1	0	0	1	0		
	SWK_DATA0_CTRL								rw	0	1	1	0	0	1	1		
	SWK_CAN_FD_CTRL								rw	0	1	1	0	1	0	0		
	SWK_OSC_TRIM_CTRL								rw	0	1	1	1	0	0	0		
	SWK_OPT_CTRL								rw	0	1	1	1	0	0	1		
	SWK_OSC_CAL_H_STAT								r	0	1	1	1	0	1	0		
	SWK_OSC_CAL_L_STAT								r	0	1	1	1	0	1	1		
	SWK_CDR_CTRL1								rw	0	1	1	1	1	0	0		
	SWK_CDR_CTRL2								rw	0	1	1	1	1	0	1		
	SWK_CER_LIMIT_H_CTRL								rw	0	1	1	1	1	1	0		
	SWK_CER_LIMIT_L_CTRL								rw	0	1	1	1	1	1	1		
Status Registers	SUP_STAT_2								rc	1	0	0	0	0	0	0	5	**Status Information Field Bit**
	SUP_STAT_1								rc	1	0	0	0	0	0	1	0	
	THERM_STAT								rc	1	0	0	0	0	1	0	1	
	DEV_STAT								rc	1	0	0	0	0	1	1	2	
	BUS_STAT_1								rc	1	0	0	0	1	0	0	3	
	BUS_STAT_2								rc	1	0	0	0	1	0	1	3	
	WK_STAT_1								rc	1	0	0	0	1	1	0	4	
	WK_STAT_2								rc	1	0	0	0	1	1	1	4	
	WK_LVL_STAT								r	1	0	0	1	0	0	0	.	
	HS_OC_OT_STAT								rc	1	0	1	0	1	0	0	6	
	HS_OL_STAT								rc	1	0	1	0	1	0	1	7	
	SWK_STAT								r	1	1	1	0	0	0	0		
	SWK_ECNT_STAT								r	1	1	1	0	0	0	1		
	SWK_CDR_STAT1								r	1	1	1	0	0	1	0		
	SWK_CDR_STAT2								r	1	1	1	0	0	1	1		
	FAM_PROD_STAT								r	1	1	1	1	1	1	0		

Figure 61 SPI Register Mapping including Selective Wake

Register Short Name	15	14	13	12	11	10	9	8	7	6...0
	Data Bit 15...8								Access Mode	Address A6...A0
	D7	D6	D5	D4	D3	D2	D1	D0		
CONTROL REGISTERS										
M_S_CTRL	MODE_1	MODE_0	VCC3_ON	VCC2_ON_1	VCC2_ON_0	VCC1_OV_RST	VCC1_RT_1	VCC1_RT_0	read/write	0000001
HW_CTRL	VCC3_V_CFG	SOFT_RESET_RO	FO_ON	VCC3_VS_UV_OFF	VCC3_LS	VCC3_OV_EN	VCC3_LS_STP_ON	CFG	read/write	0000010
WD_CTRL	CHECKSUM	WD_STM_EN_0	WD_WIN	WD_EN_WK_BUS	reserved	WD_TIMER_2	WD_TIMER_1	WD_TIMER_0	read/write	0000011
BUS_CTRL_1	LIN_FLASH	LIN_LSM	LIN_TXD_TO	LIN1_1	LIN1_0	CAN_2	CAN_1	CAN_0	read/write	0000100
BUS_CTRL_2	reserved	reserved	I_PEAK_TH	reserved	reserved	reserved	LIN2_1	LIN2_0	read/write	0000101
WK_CTRL_1	TIMER2_WK_EN	TIMER1_WK_EN	reserved	reserved	reserved	WD_STM_EN_1	reserved	reserved	read/write	0000110
WK_CTRL_2	INT_GLOBAL	reserved	WK_MEAS	reserved	reserved	WK3_EN	WK2_EN	WK1_EN	read/write	0000111
WK_PUPD_CTRL	reserved	reserved	WK3_PUPD_1	WK3_PUPD_0	WK2_PUPD_1	WK2_PUPD_0	WK1_PUPD_1	WK1_PUPD_0	read/write	0001000
WK_FLT_CTRL	reserved	reserved	WK3_FLT_1	WK3_FLT_0	WK2_FLT_1	WK2_FLT_0	WK1_FLT_1	WK1_FLT_0	read/write	0001001
TIMER1_CTRL	reserved	TIMER1_ON_2	TIMER1_ON_1	TIMER1_ON_0	reserved	TIMER1_PER_2	TIMER1_PER_1	TIMER1_PER_0	read/write	0001100
TIMER2_CTRL	reserved	TIMER2_ON_2	TIMER2_ON_1	TIMER2_ON_0	reserved	TIMER2_PER_2	TIMER2_PER_1	TIMER2_PER_0	read/write	0001101
SW_SD_CTRL	reserved	HS_OV_SD_EN	HS_UV_SD_EN	HS_OV_UV_REC	reserved	reserved	reserved	reserved	read/write	0010000
HS_CTRL_1	reserved	HS2_2	HS2_1	HS2_0	reserved	HS1_2	HS1_1	HS1_0	read/write	0010100
HS_CTRL_2	reserved	HS4_2	HS4_1	HS4_0	reserved	HS3_2	HS3_1	HS3_0	read/write	0010101
GPIO_CTRL	FO_DC_1	FO_DC_0	GPIO2_2	GPIO2_1	GPIO2_0	GPIO1_2	GPIO1_1	GPIO1_0	read/write	0010111
PWM1_CTRL	PWM1_DC_7	PWM1_DC_6	PWM1_DC_5	PWM1_DC_4	PWM1_DC_3	PWM1_DC_2	PWM1_DC_1	PWM1_DC_0	read/write	0011000
PWM2_CTRL	PWM2_DC_7	PWM2_DC_6	PWM2_DC_5	PWM2_DC_4	PWM2_DC_3	PWM2_DC_2	PWM2_DC_1	PWM2_DC_0	read/write	0011001
PWM_FREQ_CTRL	reserved	reserved	reserved	reserved	reserved	PWM2_FREQ_0	reserved	PWM1_FREQ_0	read/write	0011100
SYS_STAT_CTRL	SYS_STAT_7	SYS_STAT_6	SYS_STAT_5	SYS_STAT_4	SYS_STAT_3	SYS_STAT_2	SYS_STAT_1	SYS_STAT_0	read/write	0011110
SELECTIVE WAKE REGISTERS										
SWK_CTRL	OSC_CAL	TRIM_EN_1	TRIM_EN_0	CANTO_MASK	reserved	reserved	reserved	CFG_VAL	read/write	0100000
SWK_BTL1_CTRL	TBIT_7	TBIT_6	TBIT_5	TBIT_4	TBIT_3	TBIT_2	TBIT_1	TBIT_0	read/write	0100001
SWK_BTL2_CTRL	reserved	reserved	SP_5	SP_4	SP_3	SP_2	SP_1	SP_0	read/write	0100010
SWK_ID3_CTRL	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21	read/write	0100011
SWK_ID2_CTRL	ID20	ID19	ID18	ID17	ID16	ID15	ID14	ID13	read/write	0100100
SWK_ID1_CTRL	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5	read/write	0100101
SWK_ID0_CTRL	reserved	ID4	ID3	ID2	ID1	ID0	RTR	IDE	read/write	0100110
SWK_MASK_ID3_CTRL	MASK_ID28	MASK_ID27	MASK_ID26	MASK_ID25	MASK_ID24	MASK_ID23	MASK_ID22	MASK_ID21	read/write	0100111
SWK_MASK_ID2_CTRL	MASK_ID20	MASK_ID19	MASK_ID18	MASK_ID17	MASK_ID16	MASK_ID15	MASK_ID14	MASK_ID13	read/write	0101000
SWK_MASK_ID1_CTRL	MASK_ID12	MASK_ID11	MASK_ID10	MASK_ID9	MASK_ID8	MASK_ID7	MASK_ID6	MASK_ID5	read/write	0101001
SWK_MASK_ID0_CTRL	reserved	MASK_ID4	MASK_ID3	MASK_ID2	MASK_ID1	MASK_ID0	reserved	reserved	read/write	0101010
SWK_DLC_CTRL	reserved	reserved	reserved	reserved	DLC_3	DLC_2	DLC_1	DLC_0	read/write	0101011
SWK_DATA7_CTRL	DATA7_7	DATA7_6	DATA7_5	DATA7_4	DATA7_3	DATA7_2	DATA7_1	DATA7_0	read/write	0101100
SWK_DATA6_CTRL	DATA6_7	DATA6_6	DATA6_5	DATA6_4	DATA6_3	DATA6_2	DATA6_1	DATA6_0	read/write	0101101
SWK_DATA5_CTRL	DATA5_7	DATA5_6	DATA5_5	DATA5_4	DATA5_3	DATA5_2	DATA5_1	DATA5_0	read/write	0101110
SWK_DATA4_CTRL	DATA4_7	DATA4_6	DATA4_5	DATA4_4	DATA4_3	DATA4_2	DATA4_1	DATA4_0	read/write	0101111
SWK_DATA3_CTRL	DATA3_7	DATA3_6	DATA3_5	DATA3_4	DATA3_3	DATA3_2	DATA3_1	DATA3_0	read/write	0110000
SWK_DATA2_CTRL	DATA2_7	DATA2_6	DATA2_5	DATA2_4	DATA2_3	DATA2_2	DATA2_1	DATA2_0	read/write	0110001
SWK_DATA1_CTRL	DATA1_7	DATA1_6	DATA1_5	DATA1_4	DATA1_3	DATA1_2	DATA1_1	DATA1_0	read/write	0110010
SWK_DATA0_CTRL	DATA0_7	DATA0_6	DATA0_5	DATA0_4	DATA0_3	DATA0_2	DATA0_1	DATA0_0	read/write	0110011
SWK_CAN_FD_CTRL	reserved	reserved	DIS_ERR_CNT	RX_FILT_BYP	FD_FILTER_2	FD_FILTER_1	FD_FILTER_0	CAN_FD_EN	read/write	0110100
SELECTIVE WAKE TRIM & CONFIGURATIONS REGISTERS										
SWK_OSC_TRIM_CTRL	TRIM_OSC_7	TRIM_OSC_6	TRIM_OSC_5	TRIM_OSC_4	TRIM_OSC_3	TRIM_OSC_2	TRIM_OSC_1	TRIM_OSC_0	read/write	0111000
SWK_OPT_CTRL	RX_WK_SEL	reserved	reserved	TRIM_OSC_12	TRIM_OSC_11	TRIM_OSC_10	TRIM_OSC_9	TRIM_OSC_8	read/write	0111001
SWK_OSC_CAL_H_STAT	OSC_CAL_H_7	OSC_CAL_H_6	OSC_CAL_H_5	OSC_CAL_H_4	OSC_CAL_H_3	OSC_CAL_H_2	OSC_CAL_H_1	OSC_CAL_H_0	read	0111010
SWK_OSC_CAL_L_STAT	OSC_CAL_L_7	OSC_CAL_L_6	OSC_CAL_L_5	OSC_CAL_L_4	OSC_CAL_L_3	OSC_CAL_L_2	OSC_CAL_L_1	OSC_CAL_L_0	read	0111011
SWK_CDR_CTRL1	reserved	reserved	reserved	reserved	SELFILT_1	SELFILT_0	reserved	CDR_EN	read/write	0111100
SWK_CDR_CTRL2	reserved	reserved	reserved	reserved	reserved	reserved	SEL_OSC_CLK_1	SEL_OSC_CLK_0	read/write	0111101
SWK_CDR_LIMIT_HIGH	CDR_LIM_H_7	CDR_LIM_H_6	CDR_LIM_H_5	CDR_LIM_H_4	CDR_LIM_H_3	CDR_LIM_H_2	CDR_LIM_H_1	CDR_LIM_H_0	read/write	0111110
SWK_CDR_LIMIT_LOW	CDR_LIM_L_7	CDR_LIM_L_6	CDR_LIM_L_5	CDR_LIM_L_4	CDR_LIM_L_3	CDR_LIM_L_2	CDR_LIM_L_1	CDR_LIM_L_0	read/write	0111111
STATUS REGISTERS										
SUP_STAT_2	VCC2_OV	VS_UV	VCC3_OV	VCC3_OC	VCC3_UV	VCC3_OT	VCC1_OV	VCC1_WARN	read/clear	1000000
SUP_STAT_1	POR	VSHS_UV	VSHS_OV	VCC2_OT	VCC2_UV	VCC1_SC	VCC1_UV_FS	VCC1_UV	read/clear	1000001
THERM_STAT	reserved	reserved	reserved	reserved	reserved	TSD2	TSD1	TPW	read/clear	1000010
DEV_STAT	DEV_STAT_1	DEV_STAT_0	reserved	REF_FAIL	WD_FAIL_1	WD_FAIL_0	SPI_FAIL	FAILURE	read/clear	1000011
BUS_STAT_1	reserved	LIN1_FAIL_1	LIN1_FAIL_0	CANTO	SYSERR	CAN_FAIL_1	CAN_FAIL_0	VCAN_UV	read/clear	1000100
BUS_STAT_2	reserved	reserved	reserved	reserved	reserved	LIN2_FAIL_1	LIN2_FAIL_0	reserved	read/clear	1000101
WK_STAT_1	LIN2_WU	LIN1_WU	CAN_WU	TIMER_WU	reserved	WK3_WU	WK2_WU	WK1_WU	read/clear	1000110
WK_STAT_2	reserved	reserved	GPIO2_LVL	GPIO1_WU	reserved	reserved	reserved	reserved	read/clear	1000111
WK_LVL_STAT	SBC_DEV_LVL	CFGP	GPIO2_LVL	GPIO1_LVL	reserved	WK3_LVL	WK2_LVL	WK1_LVL	read	1001000
HS_OC_OT_STAT	reserved	reserved	reserved	reserved	HS4_OC_OT	HS3_OC_OT	HS2_OC_OT	HS1_OC_OT	read/clear	1010100
HS_OL_STAT	reserved	reserved			HS4_OL	HS3_OL	HS2_OL	HS1_OL	read/clear	1010101
SELECTIVE WAKE STATUS REGISTERS										
SWK_STAT	reserved	SYNC	reserved	reserved	CANSIL	SWK_SET	WUP	WUF	read	1110000
SWK_ECNT_STAT	reserved	reserved	ECNT_5	ECNT_4	ECNT_3	ECNT_2	ECNT_1	ECNT_0	read	1110001
SWK_CDR_STAT1	N_AVG_11	N_AVG_10	N_AVG_9	N_AVG_8	N_AVG_7	N_AVG_6	N_AVG_5	N_AVG_4	read	1110010
SWK_CDR_STAT2	N_AVG_3	N_AVG_2	N_AVG_1	N_AVG_0	reserved	reserved	reserved	reserved	read	1110011
FAMILY AND PRODUCT REGISTERS										
FAM_PROD_STAT	FAM_3	FAM_2	FAM_1	FAM_0	PROD_3	PROD_2	PROD_1	PROD_0	read	1111110

Figure 62 GD33AP236x SPI Bit Mapping including Selective Wake

16.5 SPI Control Registers

READ/WRITE Operation (see also **Chapter 16.3**):

- The 'POR / Soft Reset Value' defines the register content after POR or SBC Reset.
- The 'Restart Value' defines the register content after SBC Restart, where 'x' means the bit is unchanged.
- One 16-bit SPI command consist of two bytes:
  - the 7-bit address and one additional bit for the register access mode and
  - following the data byte
  The numbering of following bit definitions refers to the data byte and correspond to the bits D0...D7 and to the SPI bits 8...15 (see also figure before).
- There are three different bit types:
  - 'r' = READ: read only bits (or reserved bits)

- 'rw' = READ/WRITE: readable and writable bits
- 'rwh' = READ/WRITE/Hardware: readable/writable bits, which can also be modified by the SBC hardware

- Reserved bits are marked as "Reserved" and always read as "0". The respective bits shall also be programmed as "0".
- Reading a register is done byte wise by setting the SPI bit 7 to "0" (= Read Only).
- Writing to a register is done byte wise by setting the SPI bit 7 to "1".
- SPI control bits are in general not cleared or changed automatically. This must be done by the microcontroller via SPI programming. Exceptions to this behavior are stated at the respective register description and the respective bit type is marked with a 'h' meaning that the SBC is able to change the register content.

The registers are addressed wordwise.

16.5.1 General Control Registers

M_S_CTRL
Mode-and Supply Control (Address 000 0001$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 00x0 00xx$_B$

7	6	5	4	3	2	1	0
MODE_1	**MODE_0**	**VCC3_ON**	**VCC2_ON_1**	**VCC2_ON_0**	**VCC1_OV_RST**	**VCC1_RT_1**	**VCC1_RT_0**
rwh	rwh	rwh	rwh	rwh	rwh	rw	rw

Field	Bits	Type	Description
MODE	7:6	rwh	**SBC Mode Control** 00_B ,SBC Normal Mode 01_B ,SBC Sleep Mode 10_B ,SBC Stop Mode 11_B ,SBC Reset: Soft Reset is executed (configuration of RO triggering in bit **SOFT_ RESET_RO**)
VCC3_ON	5	rwh	**VCC3 Mode Control** 0_B , VCC3 OFF 1_B , VCC3 is enabled (as independent voltage regulator)
VCC2_ON	4:3	rwh	**VCC2 Mode Control** 00_B , VCC2 off 01_B , VCC2 on in Normal Mode 10_B , VCC2 on in Normal and Stop Mode 11_B , VCC2 always on (except in SBC Fail-Safe Mode)
VCC1_OV_RST	2	rwh	**VCC1 Overvoltage leading to Restart / Fail-Safe Mode enable** 0_B , **VCC1_ OV** is set in case of VCC1_OV; no SBC Restart or Fail- Safe is entered for VCC1_OV 1_B , **VCC1_OV** is set in case of VCC1_OV; depending on the device configuration SBC Restart or SBC Fail-Safe Mode is entered (see **Chapter 5.1.1**);
VCC1_RT	1:0	rw	**VCC1 Reset Threshold Control** 00_B , Vrt1 selected (highest threshold) 01_B , Vrt2 selected 10_B , Vrt3 selected 11_B , Vrt4 selected

Notes

1. It is not possible to change from Stop to Sleep Mode via SPI Command. See also the State Machine Chapter
2. After entering SBC Restart Mode, the MODE bits will be automatically set to SBC Normal Mode. The VCC2_ON bits will be automatically set to OFF after entering SBC Restart Mode and after OT.
3. The SPI output will always show the previously written state with a Write Command (what has been programmed before)

HW_CTRL
Mode-and Supply Control (Address 000 0010$_B$)
POR / Soft Reset Value: y000 y000$_B$; Restart Value: xx0x x00x$_B$

7	6	5	4	3	2	1	0
VCC3_V_CFG	SOFT_RESET_RO	FO_ON	VCC3_VS_UV_OFF	VCC3_LS	VCC3_OV_EN	VCC3_LS_STP_ON	CFG
rw	rw	rwh	rw	rw	rw	rw	rw

Field	Bits	Type	Description
VCC3_V_CFG	7	rw	**VCC3 Output Voltage Configuration (if configured as independent voltage regulator)** 0_B , VCC3 has same output voltage as VCC1 1_B , VCC3 is configured to either 3.3V or 1.8V (depending on VCC1 derivative)
SOFT_RESET_RO	6	rw	**Soft Reset Configuration** 0_B , RO will be triggered (pulled low) during a Soft Reset 1_B , No RO triggering during a Soft Reset
FO_ON	5	rwh	**Failure Output Activation (FO1..3)** 0_B , FOx not activated by software, FO can be activated by defined failures (see **Chapter 14**) 1_B , FOx activated by software (via SPI)
VCC3_VS_UV_OFF	4	rw	**VCC3 VS_UV shutdown configuration** 0_B , VCC3 will be disabled automatically at VS_UV 1_B , VCC3 will stay enabled even below VS_UV
VCC3_LS	3	rw	**VCC3 Configuration** 0_B , VCC3 operating as a stand-alone regulator 1_B , VCC3 in load sharing operation with VCC1
VCC3_OV_EN	2	rw	**VCC3 overvoltage detection control** 0_B , VCC3 overvoltage detection disabled 1_B , VCC3 overvoltage detection enabled
VCC3_LS_STP_ON	1	rw	**VCC3 Load Sharing in SBC Stop Mode configuration** 0_B , VCC3 in LS configuration during SBC Stop Mode and high- power mode: disabled 1_B , VCC3 in LS configuration during SBC Stop Mode and high- power mode: enabled

CFG	0	rw	**Configuration Select (see also Table 5)** 0_B , Depending on hardware configuration, SBC Restart or Fail- Safe Mode is reached after the 2. watchdog trigger failure (=default) - Config 3/4 1_B , Depending on hardware configuration, SBC Restart or Fail- Safe Mode is reached after the 1. watchdog trigger failure - Config 1/2

Notes

1. Clearing the FO_ON bit will not disable the FOx outputs for the case a failure occurred which triggered the FOx outputs. In this case the FOx outputs have to be disabled by clearing the FAILURE bit.

   If the FO_ON bit is set by the software then it will be cleared by the SBC after SBC Restart Mode was entered and the FOx outputs will be disabled. See also **Chapter 14** for FOx activation and deactivation.
2. After triggering a SBC Soft Reset the bits VCC3_V_CFG and VCC3_LS are not reset if they were set before,i.e. it stays unchanged, which is stated by the 'y' in the POR/Soft Reset Value. POR value: 0000 0000 and Soft Reset value: xx00 x00x
3. VCC3_LS_STP_ON: Is a combination of load sharing and VCC1 active peak in Stop mode

WD_CTRL
Watchdog Control (Address 000 0011$_B$)
POR / Soft Reset Value: 0001 0100$_B$; Restart Value: x0xx 0100$_B$

7	6	5	4	3	2	1	0
CHECKSUM	**WD_STM_ EN_0**	**WD_WIN**	**WD_EN_ WK_BUS**	**Reserved**	**WD_TIMER_2**	**WD_TIMER_1**	**WD_TIMER_0**
rw	rwh	rw	rw	r	rwh	rwh	rwh

Field	Bits	Type	Description
CHECKSUM	7	rw	**Watchdog Setting Check Sum Bit** The sum of bits 7:0 needs to have even parity (see **Chapter 15.2.3**) 0_B , Counts as 0 for checksum calculation 1_B , Counts as 1 for checksum calculation
WD_STM_ EN_0	6	rwh	**Watchdog Deactivation during Stop Mode, bit 0 (Chapter 15.2.4)** 0_B , Watchdog is active in Stop Mode 1_B , Watchdog is deactivated in Stop Mode
WD_WIN	5	rw	**Watchdog Type Selection** 0_B , Watchdog works as a Time-Out watchdog 1_B , Watchdog works as a Window watchdog
WD_EN_ WK_BUS	4	rw	**Watchdog Enable after Bus (CAN/LIN) Wake in SBC Stop Mode** 0_B , Watchdog will not start after a CAN/LINx wake 1_B , Watchdog starts with a long open window after CAN/LINx Wake
Reserved	3	r	**Reserved, always reads as 0**

WD_TIMER	2:0	rwh	**Watchdog Timer Period** 000_B , 10ms 001_B , 20ms 010_B , 50ms 011_B , 100ms 100_B , 200ms 101_B , 500ms 110_B , 1000ms 111_B , reserved

Notes

1. See also **Chapter 15.2.4** for more information on disabling the watchdog in SBC Stop Mode.
2. See **Chapter 15.2.5** for more information on the effect of the bit WD_EN_WK_BUS.
3. See **Chapter 15.2.3** for calculation of checksum.

BUS_CTRL_1
Bus Control (Address 000 0100_B)
POR / Soft Reset Value: 0010 0000_B; Restart Value: xxxyyyyy$_B$

7	6	5	4	3	2	1	0
LIN_FLASH	**LIN_LSM**	**LIN_TXD_TO**	**LIN1_1**	**LIN1_0**	**CAN_2**	**CAN_1**	**CAN_0**
rw	rw	rw	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
LIN_FLASH	7	rw	**LIN Flash Programming Mode (GD33AP2361: Reserved)** 0_B , Slope control mechanism active 1_B , Deactivation of slope control for baud rates up to 115kBaud
LIN_LSM	6	rw	**LIN Low-Slope ModeSelection (GD33AP2361: Reserved)** 0_B , LIN Normal-Mode is activated 1_B , LIN Low-Slope Mode (10.4kBaud) activated
LIN_TXD_TO	5	rw	**LIN TXD Time-Out Control (GD33AP2361: Reserved)** 0_B , TXD Time-Out feature disabled 1_B , TXD Time-Out feature enabled
LIN	4:3	rwh	**LIN-Module Modes (GD33AP2361: Reserved)** 00_B , LIN OFF 01_B , LIN is wake capable 10_B , LIN Receive Only Mode 11_B , LIN Normal Mode
CAN	2:0	rwh	**HS-CAN Module Modes** 000_B , CAN OFF 001_B , CAN is wake capable (no SWK) 010_B , CAN Receive Only Mode (no SWK) 011_B , CAN Normal Mode (no SWK) 100_B , CAN OFF 101_B , CAN is wake capable with SWK 110_B , CAN Receive Only Mode with SWK 111_B , CAN Normal Mode with SWK

Notes

1. Changes in the bits **LIN_FLASH** and **LIN_LSM** will be effective immediately once CSN goes to '1'. '
2. The reset values for the LIN and CAN transceivers are marked with 'y' because they will vary depending on the cause of change- see below.
3. see **Figure 31** and **Figure 38** for detailed state changes of LIN and CAN Transceiver for different SBC modes.
4. The bit CAN_2 is not modified by the SBC but can only be changed by the user. Therefore, the access type is 'rw' compared to bits CAN_0 and CAN_1.
5. In case SYSERR = 0 and the CAN transceiver is configured to 'x11' while going to SBC Sleep Mode, it will be automatically set to wake capable ('x01'). The SPI bits will be changed to wake capable. If configured to 'x10' and SBC Sleep Mode is entered, then the transceiver is set to wake capable, while it will stay in Receive Only Mode when it had been configured to 'x10' when going to SBC Stop Mode. If it had been configured to wake capable or OFF then the mode will remain unchanged.The Receive Only Mode has to be selected by the user before entering SBC Stop Mode. Please refer to **Chapter 5.4.4** for detailed information on the Selective Wake mode changes.
6. Failure Handling Mechanism: When the device enters Fail-Safe Mode due to a failure (TSD2, WD - Failure,...), then the wake registers **BUS_CTRL_1**, **BUS_CTRL_2** and **WK_CTRL_2** are reset to following values (=wake sources) 'xxx0 1001', '0000 0001' and 'x0x0 0111' in order to ensure that the device can be woken again.

BUS_CTRL_2

Bus Control (Address 000 0101_B)

POR / Soft Reset Value: $0000\ 0000_B$; Restart Value: $00x0\ 00yy_B$

7	6	5	4	3	2	1	0
Reserved	**Reserved**	**I_PEAK_TH**	**Reserved**	**Reserved**	**Reserved**	**LIN2_1**	**LIN2_0**
r	r	rw	r	r	r	rwh	rwh

Field	Bits	Type	Description
Reserved	7:6	r	**Reserved, always reads as 0**
I_PEAK_TH	5	rw	**VCC1 Active Peak Threshold Selection** 0_B , low VCC1 active peak threshold selected (ICC1,peak_1) 1_B , higher VCC1 active peak threshold selected (ICC1,peak_2)
Reserved	4:2	r	**Reserved, always reads as 0**
LIN2	1:0	rwh	**LIN2-Module Modes (GD33AP2361/GD33AP2362: Reserved)** 00_B , LIN2 OFF 01_B , LIN2 is wake capable 10_B , LIN2 Receive Only Mode 11_B , LIN2 Normal Mode

Notes

1. The bit **I_PEAK_TH** can be modified in SBC Init and Normal Mode. In SBC Stop Mode this bit is Read only but SPI_FAIL will not be set when trying to modify the bit in SBC STOP Mode and no INT is triggered in case **INT_GLOBAL** is set.
2. see **Figure 31** and **Figure 38** for detailed state changes of LIN and CAN Transceiver for different SBC modes
3. Failure Handling Mechanism: When the device enters Fail-Safe Mode due to a failure (TSD2, WD- Failure,...), then the wake registers **BUS_CTRL_1**, and **WK_CTRL_2** are reset to following values (=wake sources) 'xxx0 1001', and 'x0x0 0111' in order to ensure that the device can be woken again.

WK_CTRL_1

Internal Wake Input Control (Address 000 0110$_B$)

POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: xx00 0000$_B$**

7	6	5	4	3	2	1	0
TIMER2_WK_EN	TIMER1_WK_EN	Reserved	Reserved	Reserved	WD_STM_EN_1	Reserved	Reserved
rw	rw	r	r	r	rwh	r	r

Field	Bits	Type	Description
TIMER2_WK_EN	7	rw	**Timer2 Wake Source Control (for cyclic wake)** 0_B , Timer2 wake disabled 1_B , Timer2 is enabled as a wake source
TIMER1_WK_EN	6	rw	**Timer1 Wake Source Control (for cyclic wake)** 0_B , Timer1 wake disabled 1_B , Timer1 is enabled as a wake source
Reserved	5:3	r	**Reserved, always reads as 0**
WD_STM_EN_1	2	rwh	**Watchdog Deactivation during Stop Mode, bit 1 (Chapter 15.2.4)** 0_B , Watchdog is active in Stop Mode 1_B , Watchdog is deactivated in Stop Mode
Reserved	1:0	r	**Reserved, always reads as 0**

WK_CTRL_2

External Wake Source Control (Address 000 0111$_B$)

POR / Soft Reset Value: 0000 0111$_B$; **Restart Value: x0x0 0xxx$_B$**

7	6	5	4	3	2	1	0
INT_GLOBAL	Reserved	WK_MEAS	Reserved	Reserved	WK3_EN	WK2_EN	WK1_EN
rw	r	rw	r	r	rw	rw	rw

Field	Bits	Type	Description
INT_GLOBAL	7	rw	**Global Interrupt Configuration (see also Chapter 13.1)** 0_B , Only wake sources trigger INT (default) 1_B , All status information register bits will trigger INT (including all wake sources)
Reserved	6	r	**Reserved, always reads as 0**
WK_MEAS	5	rw	**WK / Measurement selection (see also Chapter 12.2.2)** 0_B , WK functionality enabled for WK1 and WK2 1_B , Measurement functionality enabled; WK1 & WK2 are disabled as wake sources, i.e. bits WK1/2_EN bits are ignored
Reserved	4:3	r	**Reserved, always reads as 0**
WK3_EN	2	rw	**WK3 Wake Source Control** 0_B , WK3 wake disabled 1_B , WK3 is enabled as a wake source

WK2_EN	1	rw	**WK2 Wake Source Control** 0_B , WK2 wake disabled 1_B , WK2 is enabled as a wake source
WK1_EN	0	rw	**WK1 Wake Source Control** 0_B , WK1 wake disabled 1_B , WK1 is enabled as a wake source

Notes

1. WK_MEAS is by default configured for standard WK functionality (WK1 and WK2). The bits WK1_EN and WK2_EN are ignored in case WK_MEAS is activated. If the bit is set to '1' then the measurement function is enabled during Normal Mode & the bits WK1_EN and WK2_EN are ignored. The bits WK1/"_LVL bits need to be ignored as well.
2. The wake sources LINx and CAN are selected in the register **BUS_CTRL_1** and **BUS_CTRL_2** by setting the respective bits to 'wake capable'
3. Failure Handling Mechanism: When the device enters Fail-Safe Mode due to a failure (TSD2, WD-Failure,...), then the wake registers **BUS_CTRL_1**, **BUS_CTRL_2** and **WK_CTRL_2** are reset to following values (=wake sources) 'xxx0 1001', '0000 0001' and 'x0x0 0111' in order to ensure that the device can be woken again.

WK_PUPD_CTRL
Wake Input Level Control (Address 000 1000_B)
POR / Soft Reset Value: 0000 0000_B; **Restart Value: 00xx $xxxx_B$**

7	6	5	4	3	2	1	0
Reserved	**Reserved**	**WK3_PUPD_1**	**WK3_PUPD_0**	**WK2_PUPD_1**	**WK2_PUPD_0**	**WK1_PUPD_1**	**WK1_PUPD_0**
r	r	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
Reserved	7:6	r	**Reserved, always reads as 0**
WK3_PUPD	5:4	rw	**WK3 Pull-Up / Pull-Down Configuration** 00_B , No pull-up / pull-down selected 01_B , Pull-down resistor selected 10_B , Pull-up resistor selected 11_B , Automatic switching to pull-up or pull-down
WK2_PUPD	3:2	rw	**WK2 Pull-Up / Pull-Down Configuration** 00_B , No pull-up / pull-down selected 01_B , Pull-down resistor selected 10_B , Pull-up resistor selected 11_B , Automatic switching to pull-up or pull-down
WK1_PUPD	1:0	rw	**WK1 Pull-Up / Pull-Down Configuration** 00_B , No pull-up / pull-down selected 01_B , Pull-down resistor selected 10_B , Pull-up resistor selected 11_B , Automatic switching to pull-up or pull-down

WK_FLT_CTRL
Wake Input Filter Time Control (Address 000 1001_B)
POR / Soft Reset Value: 0000 0000_B; **Restart Value: 00xx $xxxx_B$**

7	6	5	4	3	2	1	0
Reserved	**Reserved**	**WK3_FLT_1**	**WK3_FLT_0**	**WK2_FLT_1**	**WK2_FLT_0**	**WK1_FLT_1**	**WK1_FLT_0**
r r	r	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
Reserved	7:6	r	**Reserved, always reads as 0**
WK3_FLT	5:4	rw	**WK3 Filter Time Configuration** 00_B , Configuration A: Filter with 16µs filter time (static sensing) 01_B , Configuration B: Filter with 64µsfilter time (static sensing) 10_B , Configuration C: Filtering at the end of the on-time; a filter time of 16µs (cyclic sensing) is selected, Timer1 11_B , Configuration D: Filtering at the end of the on-time; a filter time of 16µs (cyclic sensing) is selected, Timer2
WK2_FLT	3:2	rw	**WK2 Filter Time Configuration** 00_B , Configuration A: Filter with 16µs filter time (static sensing) 01_B , Configuration B: Filter with 64µsfilter time (static sensing) 10_B , Configuration C: Filtering at the end of the on-time; a filter time of 16µs (cyclic sensing) is selected, Timer1 11_B , Configuration D: Filtering at the end of the on-time; a filter time of 16µs (cyclic sensing) is selected, Timer2
WK1_FLT	1:0	rw	**WK1 Filter Time Configuration** 00_B , Configuration A: Filter with 16µs filter time (static sensing) 01_B , Configuration B: Filter with 64µsfilter time (static sensing) 10_B , Configuration C: Filtering at the end of the on-time; a filter time of 16µs (cyclic sensing) is selected, Timer1 11_B , Configuration D: Filtering at the end of the on-time; a filter time of 16µs (cyclic sensing) is selected, Timer2

Note: When selecting a filter time configuration, the user must make sure to also assign the respective timer to at least one HS switch during cyclic sense operation

TIMER1_CTRL
Timer1 Control and Selection (Address 000 1100_B)
POR / Soft Reset Value: 0000 0000_B; **Restart Value: 0000 0000_B**

7	6	5	4	3	2	1	0
Reserved	**TIMER1_ ON_2**	**TIMER1_ ON_1**	**TIMER1_ ON_0**	**Reserved**	**TIMER1_ PER_2**	**TIMER1_ PER_1**	**TIMER1_ PER_0**
r	rwh	rwh	rwh	r	rwh	rwh	rwh

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**

TIMER1_ ON	6:4	rwh	**Timer1 On-Time Configuration** 000_B , OFF / Low (timer not running, HSx output is low) 001_B , 0.1ms on-time 010_B , 0.3ms on-time 011_B , 1.0ms on-time 100_B , 10ms on-time 101_B , 20ms on-time 110_B , OFF / HIGH (timer not running, HSx output is high) 111_B , reserved
Reserved	3	r	**Reserved, always reads as 0**
TIMER1_ PER	2:0	rwh	**Timer1 Period Configuration** 000_B , 10ms 001_B , 20ms 010_B , 50ms 011_B , 100ms 100_B , 200ms 101_B , 1s 110_B , 2s 111_B , reserved

Notes

1. A timer must be first assigned and is then automatically activated as soon as the on-time is configured.
2. If cyclic sense is selected and the HS switches are cleared during SBC Restart Mode, then also the timer settings (period and on-time) are cleared to avoid incorrect switch detection.
3. In case the timer are set as wake sources and cyclic sense is running, then both cyclic sense and cyclic wake will be active at the same time.

TIMER2_CTRL

Timer2 Control and selection (Address 000 1101_B)

POR / Soft Reset Value: 0000 0000_B; Restart Value: 0000 0000_B

7	6	5	4	3	2	1	0
Reserved	**TIMER2_ ON_2**	**TIMER2_ ON_1**	**TIMER2_ ON_0**	**Reserved**	**TIMER2_ PER_2**	**TIMER2_ PER_1**	**TIMER2_ PER_0**
r	rwh	rwh	rwh	r	rwh	rwh	rwh

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
TIMER2_ ON	6:4	rwh	**Timer2 On-Time Configuration** 000_B , OFF / Low (timer not running, HSx output is low) 001_B , 0.1ms on-time 010_B , 0.3ms on-time 011_B , 1.0ms on-time 100_B , 10ms on-time 101_B , 20ms on-time 110_B , OFF / HIGH (timer not running, HSx output is high) 111_B , reserved
Reserved	3	r	**Reserved, always reads as 0**

TIMER2_PER	2:0	rwh	**Timer2 Period Configuration** 000_B , 10ms 001_B , 20ms 010_B , 50ms 011_B , 100ms 100_B , 200ms 101_B , 1s 110_B , 2s 111_B , reserved

Notes

1. A timer must be first assigned and is then automatically activated as soon as the on-time is configured.
2. If cyclic sense is selected and the HS switches are cleared during SBC Restart Mode, then also the timer settings (period and on-time) are cleared to avoid incorrect switch detection.

SW_SD_CTRL
Switch Shutdown Control (Address 001 0000$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0xxx 0000$_B$

7	6	5	4	3	2	1	0
Reserved	**HS_OV_SD_EN**	**HS_UV_SD_EN**	**HS_OV_UV_REC**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
r	rw	rw	rw	r	r	r	r

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
HS_OV_SD_EN	6	rw	**Shutdown Disabling of HS1...4 in case of VSHS OV** 0_B , shutdown enabled in case of VSHS OV 1_B , shutdown disabled in case of VSHS OV
HS_UV_SD_EN	5	rw	**Shutdown Disabling of HS1...4 in case of VSHS UV** 0_B , shutdown enabled in case of VSHS UV 1_B , shutdown disabled in case of VSHS UV
HS_OV_UV_REC	4	rw	**Switch Recovery after Removal of VSHS OV/UV for HS1...4** 0_B , Switch recovery is disabled 1_B , Previous state before VSHS OV/UV is enabled after OV/UV condition is removed
Reserved	3:0	r	**Reserved, always reads as 0**

HS_CTRL1
High-Side Switch Control 1 (Address 001 0100$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0000 0000$_B$

7	6	5	4	3	2	1	0
Reserved	**HS2_2**	**HS2_1**	**HS2_0**	**Reserved**	**HS1_2**	**HS1_1**	**HS1_0**
rw	rwh	rwh	rwh	r	rwh	rwh	rwh

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
HS2	6:4	rwh	**HS2 Configuration** 000_B , Off 001_B , On 010_B , Controlled by Timer1 011_B , Controlled by Timer2 100_B , Controlled by PWM1 101_B , Controlled by PWM2 110_B , Reserved 111_B , Reserved
Reserved	3	r	**Reserved, always reads as 0**
HS1	2:0	rwh	**HS1 Configuration** 000_B , Off 001_B , On 010_B , Controlled by Timer1 011_B , Controlled by Timer2 100_B , Controlled by PWM1 101_B , Controlled by PWM2 110_B , Reserved 111_B , Reserved

Note: The bits for the switches are also reset in case of overcurrent and overtemperature.

HS_CTRL2
High-Side Switch Control 2 (Address 001 0101$_B$)
POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: 0000 0000$_B$**

7	6	5	4	3	2	1	0
Reserved	**HS4_2**	**HS4_1**	**HS4_0**	**Reserved**	**HS3_2**	**HS3_1**	**HS3_0**
r	rwh	rwh	rwh	r	rwh	rwh	rwh

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
HS4	6:4	rwh	**HS4 Configuration** 000_B , Off 001_B , On 010_B , Controlled by Timer1 011_B , Controlled by Timer2 100_B , Controlled by PWM1 101_B , Controlled by PWM2 110_B , Reserved 111_B , Reserved
Reserved	3	r	**Reserved, always reads as 0**

HS3	2:0	rwh	**HS3 Configuration** 000_B , Off 001_B , On 010_B , Controlled by Timer1 011_B , Controlled by Timer2 100_B , Controlled by PWM1 101_B , Controlled by PWM2 110_B , Reserved 111_B , Reserved

Note: The bits for the switches are also reset in case of overcurrent and overtemperature.

GPIO_CTRL
GPIO Configuration Control (Address 001 0111_B)
POR / Soft Reset Value: 0000 0000_B; **Restart Value: xxxx $xxxx_B$**

7	6	5	4	3	2	1	0
FO_DC_1	**FO_DC_0**	**GPIO2_2**	**GPIO2_1**	**GPIO2_0**	**GPIO1_2**	**GPIO1_1**	**GPIO1_0**
rw	rw	rw	rw	rw	rw	rw	r

Field	Bits	Type	Description
FO_DC	7:6	rw	**Duty Cycle Configuration of FO3 (if selected)** 00_B , 20% 01_B , 10% 10_B , 5% 11_B , 2.5%
GPIO2	5:3	rw	**GPIO2 Configuration** 000_B , FO3 selected 001_B , FO3 selected 010_B , FO3 selected 011_B , FO3 selected 100_B , OFF 101_B , Wake input enabled (16µs static filter) 110_B , Low-Side Switch ON 111_B , High-Side Switch ON
GPIO1	2:0	rw	**GPIO1 Configuration** 000_B , FO2 selected 001_B , FO2 selected 010_B , FO2 selected 011_B , FO2 selected 100_B , OFF 101_B , Wake input enabled (16µs static filter) 110_B , Low-Side Switch ON 111_B , High-Side Switch ON

Note: When selecting a filter time configuration, the user must make sure to also assign the respective timer to at least one HS switch during cyclic sense operation

PWM1_CTRL
PWM1 Configuration Control (Address 001 1000$_B$)
POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: xxxx xxxx$_B$**

7	6	5	4	3	2	1	0
PWM1_DC_7	PWM1_DC_6	PWM1_DC_5	PWM1_DC_4	PWM1_DC_3	PWM1_DC_2	PWM1_DC_1	PWM1_DC_0
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PWM1_DC	7:0	rw	**PWM1 Duty Cycle (bit0=LSB; bit7=MSB)** 0000 0000$_B$, 100% OFF xxxx xxxx $_B$, ON with DC fraction of 255 1111 1111$_B$, 100% ON

Note: The min. On-time during PWM is limited by the actual Ton and Toff time of the respective HS switch, e.g. the PWM setting ‘000 0001’ could not be realized.

PWM2_CTRL
PWM2 Configuration Control (Address 001 1001$_B$)
POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: xxxx xxxx$_B$**

7	6	5	4	3	2	1	0
PWM2_DC_7	PWM2_DC_6	PWM2_DC_5	PWM2_DC_4	PWM2_DC_3	PWM2_DC_2	PWM2_DC_1	PWM2_DC_0
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PWM2_DC	7:0	rw	**PWM2 Duty Cycle (bit0=LSB; bit7=MSB)** 0000 0000$_B$, 100% OFF Xxxx xxxx$_B$, ON with DC fraction of 255 1111 1111$_B$, 100% ON

Note: The min. On-time during PWM is limited by the actual Ton and Toff time of the respective HS switch, e.g. the PWM setting ‘000 0001’ could not be realized.

PWM_FREQ_CTRL
PWM Frequency Configuration Control (Address 001 1100$_B$)
POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: 0000 0x0x$_B$**

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	PWM2_FREQ	Reserved	PWM1_FREQ
r	r	r	r	r	rw	r	rw

Field	Bits	Type	Description

Reserved	7:3	r	**Reserved, always reads as 0**
PWM2_ FREQ	2	rw	**PWM2 Frequency Selection** 0_B , 200Hz configuration 1_B , 400Hz configuration
Reserved	1	r	**Reserved, always reads as 0**
PWM1_ FREQ	0	rw	**PWM1 Frequency Selection** 0_B , 200Hz configuration 1_B , 400Hz configuration

Notes

1. The min. On-time during PWM is limited by the actual Ton and Toff time of the respective HS switch, e.g. the PWM setting '000 0001' could not be realized.
2. The actual PWM frequency correlates with the internal clock tolerance as specified in parameter $\mathbf{f_{CLKSBC}}$.

SYS_STATUS_CTRL
System Status Control (Address 001 1110$_B$)
POR Value: 0000 0000$_B$; **Reset Value/Soft Reset Value: xxxx xxxx$_B$**

7	6	5	4	3	2	1	0
SYS_STAT_7	**SYS_STAT_6**	**SYS_STAT_5**	**SYS_STAT_4**	**SYS_STAT_3**	**SYS_STAT_2**	**SYS_STAT_1**	**SYS_STAT_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
SYS_STAT	7:0	rw	**System Status Control Byte (bit0=LSB; bit7=MSB)** Dedicated byte for system configuration, access only by microcontroller. Cleared after power up and Soft Reset

Notes

1. The **SYS_STATUS_CTRL** register is an exception for the default values, i.e. it will keep its configured value also after a Soft Reset.
2. This byte is intended for storing system configurations of the ECU by the microcontroller and is only accessible in SBC Normal Mode. The byte is not accessible by the SBC and is also not cleared after Fail-Safe or SBC Restart Mode. It allows the microcontroller to quickly store system configuration without losing the data

16.5.2 Selective Wake Control Registers

SWK_CTRL
CAN Selective Wake Control (Address 010 0000$_B$)
POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: xxxx 0000$_B$**

7	6	5	4	3	2	1	0
OSC_CAL	**TRIM_EN_1**	**TRIM_EN_0**	**CANTO_ MASK**	**Reserved**	**Reserved**	**Reserved**	**CFG_VAL**
rw	rw	rw	rw	r	r	r	rwh

Field	Bits	Type	Description

OSC_CAL	7	rw	**Oscillator Calibration Mode** 0_B , Oscillator Calibration is disabled 1_B , Oscillator Calibration is enabled
TRIM_EN	6:5	rw	**(Un)locking mechanism of oscillator recalibration** 00_B , locked 01_B , locked 10_B , locked 11_B , unlocked
CANTO_ MASK	4	rw	**CAN Time Out Masking** 0_B , CAN time-out is masked - no interrupt (on pin INT) is triggered 1_B , CAN time-out is signaled on INT
Reserved	3:1	r	**Reserved, always reads as 0**
CFG_VAL	0	rwh	**SWK Configuration valid** 0_B , Configuration is not valid (SWK not possible) 1_B , SWK configuration valid, needs to be set to enable SWK

Notes

1. TRIM_EN unlocks the oscillation calibration mode. Only the bit combination '11' is the valid unlock. The pin TXDCAN is used for oscillator synchronisation (trimming).
2. The microcontroller needs to validate the SWK configuration and set 'CFG_VAL' to '1'. The SBC will only enable SWK if CFG_VAL' to '1'. The bit will be cleared automatically by the SBC after a wake up or POR or if a SWK configuration data is changed by the microcontroller.
3. CANTO bit will only be updated inside BUS_STAT while CAN_2 is set. Therefore, an interrupt is only signaled upon occurrence of CANTO while CAN_2 (SWK is enabled) is set in SBC Normal and Stop Mode.
4. TRIM_EN also unlocks the writing to the SWK_OPT_CTRL register in order to enable the alternate low-power Receiver for Selective wake to optimize the quiescent current consumption. Only the bit combination '11'
   unlocks the calibrations / configurations.
5. In SBC stop-mode, any write command to a CAN or SWK configuration register will lead to CFG_VAL be set to '0' (SWK becomes invalid).

SWK_BTL1_CTRL
SWK Bit Timing Logic Control1 (Address 010 0001$_B$)
POR / Soft Reset Value: 1010 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
TBIT_7	**TBIT_6**	**TBIT_5**	**TBIT_4**	**TBIT_3**	**TBIT_2**	**TBIT_1**	**TBIT_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
TBIT	7:0	rw	**Number of Time Quanta in a Bit Time** Represents the number of time quanta in a bit time. Quanta is depending on **SEL_OSC_CLK**<1:0> from the **SWK_CDR_CTRL2** register.

SWK_BTL2_CTRL
SWK Bit Timing Control2 (Address 010 0010$_B$)
POR / Soft Reset Value: 0011 0011$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
reserved	reserved	SP_5	SP_4	SP_3	SP_2	SP_1	SP_0
r	r	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
Reserved	7:6	r	**Reserved, always reads as 0**
SP	5:0	rw	**Sampling Point Position** Represents the sampling point position (fractional number < 1). Example: 0011 0011 = 0.796875 (~80%)

SWK_ID3_CTRL
SWK WUF Identifier bits 28...21 (Address 010 0011$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ID28_21	7:0	rw	**WUF Identifier Bits 28...21**

Note: Please note the configuration of the standard identifier and extended identifier. The standard identifier is configured to the bits ID18...ID28

SWK_ID2_CTRL
SWK WUF Identifier bits 20...13 (Address 010 0100$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
ID20	ID19	ID18	ID17	ID16	ID15	ID14	ID13
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ID20_13	7:0	rw	**WUF Identifier Bits 20...13**

SWK_ID1_CTRL
SWK WUF Identifier bits 12...5 (Address 010 0101$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0

ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ID12_5	7:0	rw	**WUF Identifier Bits 12...5**

SWK_ID0_CTRL
SWKWUF Identifier bits 4...0 (Address 010 0110$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0xxx xxxx$_B$

7	6	5	4	3	2	1	0
reserved	ID4	ID3	ID2	ID1	ID0	RTR	IDE
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
ID4_0	6:2	rw	**WUF Identifier Bits 4..0**
RTR	1	rw	**Remote Transmission Request Field (acc. ISO 11898-1)** 0_B , Normal Data Frame 1_B , Remote Transmission Request
IDE	0	rw	**Identifier Extension Bit** 0_B , Standard Identifier Length (11 bit) 1_B , Extended Identifier Length (29 bit)

Note: The setting RTR = 1 is not allowed for wake-up frames according to the ISO11898-2:2016

SWK_MASK_ID3_CTRL
SWKWUF Identifier Mask bits 28...21 (Address 010 0111$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
MASK_ID28	MASK_ID27	MASK_ID26	MASK_ID25	MASK_ID24	MASK_ID23	MASK_ID22	MASK_ID21
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
MASK_ID28_21	7:0	rw	**WUF Identifier Mask Bits 28...21** 0_B , Unmasked - bit is ignored 1_B , Masked - bit is compared in CAN frame

Note: Masking WUF bits is done by setting the respective MASK bit to '1'

SWK_MASK_ID2_CTRL
SWKWUF Identifier Mask bits 20...13 (Address 010 1000$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
MASK_ID20	MASK_ID19	MASK_ID18	MASK_ID17	MASK_ID16	MASK_ID15	MASK_ID14	MASK_ID13
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
MASK_ID20_13	7:0	rw	**WUF Identifier Mask Bits 20...13** 0_B , Unmasked - bit is ignored 1_B , Masked - bit is compared in CAN frame

SWK_MASK_ID1_CTRL
SWKWUF Identifier Mask bits 12...5 (Address 010 1001$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
MASK_ID12	MASK_ID11	MASK_ID10	MASK_ID9	MASK_ID8	MASK_ID7	MASK_ID6	MASK_ID5
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
MASK_ID12_5	7:0	rw	**WUF Identifier Mask Bits 12...5** 0_B , Unmasked - bit is ignored 1_B , Masked - bit is compared in CAN frame

SWK_MASK_ID0_CTRL
SWKWUF Identifier bits 4...0 (Address 010 1010$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0xxxxx00$_B$

7	6	5	4	3	2	1	0
Reserved	MASK_ID4	MASK_ID3	MASK_ID2	MASK_ID1	MASK_ID0	Reserved	Reserved
rw	rw	rw	rw	rw	rw	r	r

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
MASK_ID4_0	6:2	rw	**WUF Identifier MASK Bits 4..0** 0_B , Unmasked - bit is ignored 1_B , Masked - bit is compared in CAN frame
Reserved	1:0	r	**Reserved, always reads as 0**

SWK_DLC_CTRL
SWK Frame Data Length Code Control (Address 010 1011$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0000 xxxx$_B$

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	DLC_3	DLC_2	DLC_1	DLC_0
r	r	r	r	rw	rw	rw	rw

Field	Bits	Type	Description
Reserved	7:4	r	**Reserved, always reads as 0**
DLC	3:0	rw	**Payload length in number of bytes** 0000$_B$, Frame Data Length = 0 or cleared 0001$_B$, Frame Data Length = 1 0010$_B$, Frame Data Length = 2 0011$_B$, Frame Data Length = 3 0100$_B$, Frame Data Length = 4 0101$_B$, Frame Data Length = 5 0110$_B$, Frame Data Length = 6 0111$_B$, Frame Data Length = 7 from 1000B to 1111B Frame Data Length = 8

Note: The number of bytes in the data field has to be indicated by the DLC. The DLC consists of four bits. The admissible number of data bytes for a data frame ranges from zero to eight. DLCs in the range of zero to seven shall indicate data fields of length of zero to seven bytes. DLCs in the range from eight to fifteen indicate data fields of length of eight byte. The configured DLC value has to match bit by bit with the DLC in the received wake-up frame (refer also to **Chapter 5.4.2.3**).

SWK_DATA7_CTRL
SWK Data7 Register (Address 010 1100$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
DATA7_7	DATA7_6	DATA7_5	DATA7_4	DATA7_3	DATA7_2	DATA7_1	DATA7_0
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
DATA7	7:0	rw	**Data7 byte content(bit0=LSB; bit7=MSB)**

SWK_DATA6_CTRL
SWK Data6 Register (Address 010 1101$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0

DATA6_7	DATA6_6	DATA6_5	DATA6_4	DATA6_3	DATA6_2	DATA6_1	DATA6_0
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
DATA6	7:0	rw	Data6 byte content (bit0=LSB; bit7=MSB)

SWK_DATA5_CTRL
SWK Data5 Register (Address 010 1110$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
DATA5_7	DATA5_6	DATA5_5	DATA5_4	DATA5_3	DATA5_2	DATA5_1	DATA5_0
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
DATA5	7:0	rw	Data5 byte content (bit0=LSB; bit7=MSB)

SWK_DATA4_CTRL
SWK Data4 Register (Address 010 1111$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
DATA4_7	DATA4_6	DATA4_5	DATA4_4	DATA4_3	DATA4_2	DATA4_1	DATA4_0
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
DATA4	7:0	rw	Data4 byte content (bit0=LSB; bit7=MSB)

SWK_DATA3_CTRL
SWK Data3 Register (Address 011 0000$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
DATA3_7	DATA3_6	DATA3_5	DATA3_4	DATA3_3	DATA3_2	DATA3_1	DATA3_0
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
DATA3	7:0	rw	Data3 byte content (bit0=LSB; bit7=MSB)

SWK_DATA2_CTRL
SWK Data2 Register (Address 011 0001$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
DATA2_7	DATA2_6	DATA2_5	DATA2_4	DATA2_3	DATA2_2	DATA2_1	DATA2_0
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
DATA2	7:0	rw	Data2 byte content (bit0=LSB; bit7=MSB)

SWK_DATA1_CTRL
SWK Data1 Register (Address 011 0010$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
DATA1_7	DATA1_6	DATA1_5	DATA1_4	DATA1_3	DATA1_2	DATA1_1	DATA1_0
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
DATA1	7:0	rw	Data1 byte content (bit0=LSB; bit7=MSB)

SWK_DATA0_CTRL
SWK Data0 Register (Address 011 0011$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
DATA0_7	DATA0_6	DATA0_5	DATA0_4	DATA0_3	DATA0_2	DATA0_1	DATA0_0
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
DATA0	7:0	rw	Data0 byte content (bit0=LSB; bit7=MSB)

SWK_CAN_FD_CTRL
CAN FD Configuration Control Register (Address 011 0100$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 00xx xxxx$_B$

7	6	5	4	3	2	1	0
Reserved	Reserved	DIS_ERR_CNT	RX_FILT_BYP	FD_FILTER_2	FD_FILTER_1	FD_FILTER_0	CAN_FD_EN
r	r	rwh	rw	rw	rw	rw	rw

Field	Bits	Type	Description

Reserved	7:6	r	**Reserved, always reads as 0**
DIS_ERR_ CNT	5	rwh	**Error Counter Disable Function** 0_B , Error Counter is enabled during SWK 1_B , Error counter is disabled during SWK only if CAN_FD_EN = '1'
RX_FILT_ BYP	4	rw	**RX Receiver Filter Bypass** 0_B , RX Filter not bypassed 1_B , RX Filter bypassed
FD_FILTER	3:1	rw	**CAN FD Dominant Filter Time** 000_B , 50 ns 001_B , 100 ns 010_B , 150 ns 011_B , 200 ns 100_B , 250 ns 101_B , 300 ns 110_B , 350 ns 111_B , 775 ns
CAN_FD_ EN	0	rw	**Enable CAN FD Tolerant Mode** 0_B , CAN FD Tolerant Mode disabled 1_B , CAN FD Tolerant Mode enabled

Note: The bit **RX_FILT_ BYP** is bypassing the analog filter in the CAN receiver path; The **FD_FILTER** is not in the analog path of the CAN receiver and is not bypassed.

Note: **DIS_ERR_ CNT** is cleared by the SBC at tsilence expiration.

16.5.3 Selective Wake Trimming and Calibration Control Registers

SWK_OSC_TRIM_CTRL
SWK Oscillator Trimming Register (Address 011 1000_B)
POR / Soft Reset Value: xxxx $xxxx_B$; Restart Value: xxxx $xxxx_B$

7	6	5	4	3	2	1	0
TRIM_OSC_7	**TRIM_OSC_6**	**TRIM_OSC_5**	**TRIM_OSC_4**	**TRIM_OSC_3**	**TRIM_OSC_2**	**TRIM_OSC_1**	**TRIM_OSC_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
TRIM_OSC	7:0	rw	**Oscillator trimming (bit0=LSB; bit7=MSB);** **(only writable if TRIM_EN = '11')**

Note: TRIM_OSC[0:4] represent the 32-steps fine trimming range with a monotonous behavior from slower to faster frequency. The step width is ~0.25MHz.
TRIM_OSC[5:7] are modifying the oscillator temperature coefficient. It is strongly recommended to not change these values.
Due to CDR functionality, it is not required to change these values.

SWK_OPT_CTRL

Selective Wake Options Register (Address 011 1001$_B$)

POR / Soft Reset Value: 000x xxxx$_B$; Restart Value: x00x xxxx$_B$

7	6	5	4	3	2	1	0
RX_WK_SEL	Reserved	Reserved	TRIM_OSC_12	TRIM_OSC_11	TRIM_OSC_10	TRIM_OSC_9	TRIM_OSC_8
rw	r	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
RX_WK_SEL	7	rw	**SWK Receiver selection (only accessible if TRIM_EN = '11')** 0_B , Low-Power Receiver selected during SWK 1_B , Standard Receiver selected during SWK
Reserved	6:5	r	**Reserved, always reads as 0**
TRIM_OSC	4:0	rw	**Oscillator trimming (bit8=LSB; bit12=MSB);** **(only writable if TRIM_EN = '11')**

Important: If the RX_WK_SEL bit is changed, then it must be ensured that the values of TRIM_OSC [8:12] bits remain unchanged to avoid a change of oscillator frequency.
TRIM_OSC[8:12] represent the 32-steps coarse trimming range, which is not monotonous. It is not recommended to change these values.

SWK_OSC_CAL_H_STAT

SWK Oscillator Calibration High Register (Address 011 1010$_B$)

POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
OSC_CAL_H_7	OSC_CAL_H_6	OSC_CAL_H_5	OSC_CAL_H_4	OSC_CAL_H_3	OSC_CAL_H_2	OSC_CAL_H_1	OSC_CAL_H_0
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
OSC_CAL_H	7:0	r	**Oscillator Calibration High Register**

SWK_OSC_CAL_L_STAT

SWK Oscillator Calibration Low Register (Address 011 1011$_B$)

POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
OSC_CAL_L_7	OSC_CAL_L_6	OSC_CAL_L_5	OSC_CAL_L_4	OSC_CAL_L_3	OSC_CAL_L_2	OSC_CAL_L_1	OSC_CAL_L_0
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
OSC_CAL_L	7:0	r	**Oscillator Calibration Low Register**

SWK_CDR_CTRL1
CDR Control 1 Register (Address 011 1100$_B$)
POR / Soft Reset Value: 0000 0100$_B$; Restart Value: 0000 xx0x$_B$

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	SEL_FILT_1	SEL_FILT_0	Reserved	CDR_EN
r	r	r	r	rw	rw	r	rw

Field	Bits	Type	Description
Reserved	7:4	r	**Reserved, always reads as 0**
SEL_FILT	3:2	rw	**Select Time Constant of Filter** 00_B , Time constant 8 01_B , Time constant 16 (default) 10_B , Time constant 32 11_B , adapt distance between falling edges 2, 3 bit: Time constant 32 distance between f. edges 4, 5, 6, 7, 8 bit: Time constant 16 distance between falling edges 9, 10 bit: Time constant 8
Reserved	1	r	**Reserved, always reads as 0**
CDR_EN	0	rw	**Enable CDR** 0_B , CDR disabled 1_B , CDR enabled

SWK_CDR_CTRL2
CDR Control 2Register (Address 011 1101$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0000 00xx$_B$

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SEL_OSC_CLK_1	SEL_OSC_CLK_0
r	r	r	r	r	r	rw	rw

Field	Bits	Type	Description
Reserved	7:2	r	**Reserved, always reads as 0**
SEL_OSC_CLK	1:0	rw	**Input Frequency for CDR module** See **Table 37** and **Table 38**.

Table 37 Frequency Settings of Internal Clock for the CDR

SEL_OSC_CLK[1:0]	int. Clock for CDR
00	80 MHz
01	40 MHz
10	20 MHz
11	10 MHz

Table 38 Recommended CDR Settings for Different Baud Rates

SEL_OSC_CLK [1:0]	Baudrate	SWK_BTL1_CTRLValue	SWK_CDR_LIMIT_HIGH _CTRLValue	SWK_CDR_LIMIT_LOW _ CTRLValue
00	500k	1010 0000	1010 1000	1001 1000
01	500k	0101 0000	0101 0100	0100 1100
10	500k	CDR Setting not recommended for this baudrate due to insufficient precision		

Table 38 Recommended CDR Settings for Different Baud Rates (cont'd)

SEL_OSC_CLK [1:0]	Baudrate	SWK_BTL1_CTRL Value	SWK_CDR_LIMIT_HIGH _CTRL Value	SWK_CDR_LIMIT_LOW_ CTRL Value
11	500k	CDR Setting not recommended for this baudrate due to insufficient precision		
00	250k	CDR Setting not to be used due to excessive time quanta (counter overflow)		
01	250k	1010 0000	1010 1000	1001 1000
10	250k	0101 0000	0101 0100	0100 1100
11	250k	CDR Setting not recommended for this baudrate due to insufficient precision		
00	125k	CDR Setting not to be used due to excessive time quanta (counter overflow)		
01	125k	CDR Setting not to be used due to excessive time quanta (counter overflow)		
10	125k	1010 0000	1010 1000	1001 1000
11	125k	0101 0000	0101 0100	0100 1100

SWK_CDR_LIMIT_HIGH_CTRL
SWK CDR Upper Limit Control (Address 011 1110$_B$)
POR / Soft Reset Value: 1010 1000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
CDR_LIM_ H_7	CDR_LIM_ H_6	CDR_LIM_ H_5	CDR_LIM_ H_4	CDR_LIM_ H_3	CDR_LIM_ H_2	CDR_LIM_ H_1	CDR_LIM_ H_0
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
CDR_LIM_H	7:0	rw	**Upper Bit Time Detection Range of Clock and Data Recovery** **SWK_BTL1_CTRL** values > + 5% will be clamped

SWK_CDR_LIMIT_LOW_CTRL
SWK CDR Lower Limit Control (Address 011 1111$_B$)
POR / Soft Reset Value: 1001 1000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
CDR_LIM_ L_7	CDR_LIM_ L_6	CDR_LIM_ L_5	CDR_LIM_ L_4	CDR_LIM_ L_3	CDR_LIM_ L_2	CDR_LIM_ L_1	CDR_LIM_ L_0
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
CDR_LIM_L	7:0	rw	**Lower Bit Time Detection Range of Clock and Data Recovery** **SWK_BTL1_CTRL** values < - 5% will be clamped

16.6 SPI Status Information Registers

READ/CLEAR Operation (see also **Chapter 16.3**):

- One 16-bit SPI command consist of two bytes:
  - the 7-bit address and one additional bit for the register access mode and
  - following the data byte
  The numbering of following bit definitions refers to the data byte and correspond to the bits D0...D7 and to the SPI bits 8...15 (see also figure).
- There are two different bit types:
  - 'r' = READ: read only bits (or reserved bits)
  - 'rc' = READ/CLEAR: readable and clearable bits
- Reading a register is done byte wise by setting the SPI bit 7 to "0" (= Read Only)
- Clearing a register is done byte wise by setting the SPI bit 7 to "1"
- SPI status registers are in general not cleared or changed automatically (an exception are the **WD_FAIL** bits). This must be done by the microcontroller via SPI command

The registers are addressed wordwise

16.6.1 General Status Registers

SUP_STAT_2
Supply Voltage Fail Status (Address 100 0000$_B$)
POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: xxxx xxxx$_B$**

7	6	5	4	3	2	1	0
VCC2_OV	VS_UV	VCC3_OV	VCC3_OC	VCC3_UV	VCC3_OT	VCC1_OV	VCC1_WARN
rc	rc	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
VCC2_OV	7	rc	**VCC2 Overvoltage Detection** 0_B , No VCC2 overvoltage warning 1_B , VCC2 overvoltage detected
VS_UV	6	rc	**VS Undervoltage Detection ($V_{S,UV}$)** 0_B , No VS undervoltage detected 1_B , VS undervoltage detected
VCC3_OV	5	rc	**VCC3 Overvoltage Detection** 0_B , No VCC3 overvoltage warning 1_B , VCC3 overvoltage detected
VCC3_OC	4	rc	**VCC3 Overcurrent Detection** 0_B , No OC 1_B , OC detected
VCC3_UV	3	rc	**VCC3 Undervoltage Detection** 0_B , No VCC3 UV detection 1_B , VCC3 UV Fail detected
VCC3_OT	2	rc	**VCC3 Overtemperature Detection** 0_B , No overtemperature 1_B , VCC3 overtemperature detected
VCC1_OV	1	rc	**VCC1 Overvoltage Detection ($V_{CC1,OV,r}$)** 0_B , No VCC1 overvoltage warning 1_B , VCC1 overvoltage detected

VCC1_ WARN	0	rc	**VCC1 Undervoltage Prewarning ($V_{PW,f}$)** 0_B , No VCC1 undervoltage prewarning 1_B , VCC1 undervoltage prewarning detected

Notes

1. The VCC1 undervoltage prewarning threshold $V_{PW,f}$ $N_{PW,r}$ is a fixed threshold and independent of the VCC1 undervoltage reset thresholds.

SUP_STAT_1
Supply Voltage Fail Status (Address 100 0001_B)
POR / Soft Reset Value: y000 0000_B; **Restart Value: xxxx xx0x$_B$**

7	6	5	4	3	2	1	0
POR	**VSHS_UV**	**VSHS_OV**	**VCC2_OT**	**VCC2_UV**	**VCC1_SC**	**VCC1_UV_FS**	**VCC1_UV**
rc	rc	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
POR	7	rc	**Power-On Reset Detection** 0_B , No POR 1_B , POR occurred
VSHS_UV	6	rc	**VSHS Undervoltage Detection ($V_{SHS,UVD}$)** 0_B , No VSHS-UV 1_B , VSHS-UV detected
VSHS_OV	5	rc	**VSHS Overvoltage Detection ($V_{SHS,OVD}$)** 0_B , NoVSHS-OV 1_B , VSHS-OV detected
VCC2_OT	4	rc	**VCC2 Overtemperature Detection** 0_B , No overtemperature 1_B , VCC2 overtemperature detected
VCC2_UV	3	rc	**VCC2 Undervoltage Detection ($V_{CC2,UV,f}$)** 0_B , No VCC2 undervoltage 1_B , VCC2 undervoltage detected
VCC1_SC	2	rc	**VCC1 Short to GND Detection (<Vrtx fort>4ms after switch on)** 0_B , No short 1_B , VCC1 short to GND detected
VCC1_UV _FS	1	rc	**VCC1 UV-Detection (due to Vrtx reset)** 0_B , No Fail-Safe Mode entry due to 4th consecutive VCC1_UV 1_B , Fail-Safe Mode entry due to 4th consecutive VCC1_UV
VCC1_UV	0	rc	**VCC1 UV-Detection (due to Vrtx reset)** 0_B , No VCC1_UV detection 1_B , VCC1 UV-Fail detected

Notes

1. The MSB of the POR/Soft Reset value is marked as 'y': the default value of the POR bit is set after Power-on reset (POR value = 1000 0000). However it will be cleared after a SBC Soft Reset command (Soft Reset value = 0000 0000).
2. During Sleep Mode, the bits VCC1_SC, VCC1_OV and VCC1_UV will not be set when VCC1 is off

3. The VCC1_UV bit is never updated in SBC Restart Mode, in SBC Init Mode it is only updated after RO was released for the first time, it is always updated in SBC Normal and Stop Mode, and it is always updated in any SBC modes in a VCC1_SC condition (after VCC1_UV = 1 for >4ms).

THERM_STAT
Thermal Protection Status (Address 100 0010$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0000 0xxx$_B$

7	6	5	4	3	2	1	0
Reserved	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**TSD2**	**TSD1**	**TPW**
r	r	r	r	r	rc	rc	rc

Field	Bits	Type	Description
Reserved	7:3	r	**Reserved, always reads as 0**
TSD2	2	rc	**TSD2 Thermal Shut-Down Detection** 0_B , No TSD2 event 1_B , TSD2 OT detected - leading to SBC Fail-Safe Mode
TSD1	1	rc	**TSD1 Thermal Shut-Down Detection** 0_B , No TSD1 fail 1_B , TSD1 OT detected
TPW	0	rc	**Thermal Pre Warning** 0_B , No Thermal Pre warning 1_B , Thermal Pre warning detected

Note: TSD1 and TSD2 are not reset automatically, even if the temperature pre warning or TSD1 OT condition is not present anymore. Also TSD2 is not reset.

DEV_STAT
Device Information Status (Address 100 0011$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xx0x xxxx$_B$

7	6	5	4	3	2	1	0
DEV_STAT_1	**DEV_STAT_0**	**Reserved**	**REF_FAIL**	**WD_FAIL_1**	**WD_FAIL_0**	**SPI_FAIL**	**FAILURE**
rc	rc	r	rc	rh	rh	rc	rc

Field	Bits	Type	Description
DEV_STAT	7:6	rc	**Device Status before Restart Mode** 00_B , Cleared (Register must be actively cleared) 01_B , Restart due to failure (WD fail, TSD2,VCC1_UV); also after a wake from Fail-Safe Mode 10_B , Sleep Mode 11_B , Reserved
Reserved	5	r	**Reserved, always reads as 0**
REF_FAIL	4	rc	**Internal Reference Fail** 0_B , No internal reference fail 1_B , Internal reference fail detected

WD_FAIL	3:2	rh	**Number of WD-Failure Events (1/2 WD failures depending on CFG)** 00_B , No WD Fail 01_B , 1x WD Fail, FOx activation - Config 2 selected 10_B , 2x WD Fail, FOx activation - Config 1 / 3 / 4 selected 11_B , Reserved (never reached)
SPI_FAIL	1	rc	**SPI Fail Information** 0_B , No SPI fail 1_B , Invalid SPI command detected
FAILURE	0	rc	**Activation of Fail Output FO** 0_B , No Failure 1_B , Failure occurred

Notes

1. The bits **DEV_STAT** show the status of the device before it went through Restart. Either the device came from regular Sleep Mode (‘10’) or a failure (‘01’ - SBC Restart or SBC Fail-Safe Mode: WD fail, TSD2 fail, VCC_UV fail or VCC1_OV if bit **VCC1_OV_RST** is set) occurred. Failure is also an illegal command from SBC Stop to SBC Sleep Mode or going to SBC Sleep Mode without activation of any wake source. Coming from SBC Sleep Mode (‘10’) will also be shown if there was a trial to enter SBC Sleep Mode without having cleared all wake flags before.
2. The **WD_FAIL** bits are configured as a counter and are the only status bits, which are cleared automatically by the SBC. They are cleared after a successful watchdog trigger and when the watchdog is stopped (also in SBC Sleep and Fail-Safe Mode unless it was reached due to a watchdog failure). See also **Chapter 14.1.**
3. The SPI_FAIL bit is cleared only by SPI command
4. In case of Config 2/4 the WD_Fail counter is frozen in case of WD trigger failure until a successful WD trigger.
5. If CFG = ‘0’ then a 1st watchdog failure will not trigger the FO outputs or the FAILURE bit but only force the SBC into SBC Restart Mode.
6. In case any internal reference fails, **REF_FAIL** will be set and SBC will go to Fail-Safe Mode.

BUS_STAT_1

Bus Communication Status (Address 100 0100_B)

POR / Soft Reset Value: $0000\ 0000_B$; **Restart Value: $0xxx\ xxxx_B$**

7	6	5	4	3	2	1	0
Reserved	**LIN1_FAIL_1**	**LIN1_FAIL_0**	**CANTO**	**SYSERR**	**CAN_FAIL_1**	**CAN_FAIL_0**	**VCAN_UV**
r	rc	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
LIN1_FAIL	6:5	rc	**LIN1 Failure Status (GD33AP2361: Reserved)** 00_B , No error 01_B , LIN1 TSD 10_B , LIN1_TXD_DOM: TXD dominant time out for more than 20ms 11_B , LIN1_BUS_DOM: BUS dominant time out for more than 20ms
CANTO	4	rc	**CAN Time Out Detection** 0_B , Normal operation 1_B , CAN Time Out detected

SYSERR	3	rc	**SWK System Error** 0_B , Selective Wake Mode is possible 1_B , System Error detected, SWK enabling not possible
CAN_FAIL	2:1	rc	**CAN Failure Status** 00_B , No error 01_B , CANTSD shutdown 10_B , CAN_TXD_DOM: TXD dominant time out for longer than $t_{TxD\_CAN\_TO}$ 11_B , CAN_BUS_DOM: BUS dominant time out for longer than $t_{TxD\_CAN\_TO}$
VCAN_UV	0	rc	**Undervoltage CAN Bus Supply** 0_B , Normal operation 1_B , CAN Supply undervoltage detected. Transmitter disabled

Notes

1. CAN and LIN Recovery Conditions:
   1) TXD Time Out: TXD goes HIGH or transmitter is set to wake capable or switched off;
   2) Bus dominant time out: Bus will become recessive or transceiver is set to wake capable or switched off.
   3) Supply undervoltage: as soon as the threshold is crossed again,i.e. VSHS>VS_UV for LIN and VCAN > VCAN_UV for CAN
   4) In all cases (also for TSD shutdown): to enable the Bus transmission again, TXD needs to be HIGH for a certain time (transmitter enable time).
2. The VCAN_UV comparator is enabled if the mode bit CAN_1 = '1',i.e. in CAN Normal or CAN Receive Only Mode.
3. CANTO will be set only if CAN2 = 1 (=SWK Mode enabled). It will be set as soon as CANSIL was set and will stay set even in CANSIL it is reset. An interrupt is issued in SBC Stop- and SBC Normal Mode as soon as CANTO is set and the interrupt is not masked out,i.e. CANTO_MASK must be set to 1.
4. The SYSERR Flag is set in case of a configuration error and in case of an error counter overflow (n>32). It is only updated if SWK is enabled (CAN_2 = '1'). See also **Chapter 5.4.3**.
5. CANTO is set asynchronously to the INT pulse. In order to prevent undesired clearing of CANTO and thus possibly missing this interrupt, the bit will be prevented from clearing (i.e. cannot be cleared) until the next falling edge of INT.

BUS_STAT_2
Bus Communication Status (Address 100 0101_B)
POR / Soft Reset Value: 0000 0000_B; Restart Value: 0000 $0xx0_B$

7	6	5	4	3	2	1	0
Reserved	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**LIN2_FAIL_1**	**LIN2_FAIL_0**	**Reserved**
r	r	r	r	r	rc	rc	r

Field	Bits	Type	Description
Reserved	7:3	r	**Reserved, always reads as 0**
LIN2_FAIL	2:1	rc	**LIN2 Failure Status (GD33AP2361/GD33AP2362: Reserved)** 00_B , No error 01_B , LIN2 TSD shutdown 10_B , LIN2_TXD_DOM: TXD dominant time out for more than 20ms 11_B , LIN2_BUS_DOM: BUS dominant time out for more than 20ms
Reserved	0	r	**Reserved, always reads as 0**

Note: CAN and LINx Recovery Conditions:

1) TXD Time Out: TXD goes High or transmitter is set to wake capable or switched off;
2) Bus dominant time out: Bus will become recessive or transceiver is set to wake capable or switched off.
3) Supply undervoltage: as soon as the threshold is crossed again,i.e. VSHS > VS_UV for LINx and VCAN > VCAN_UV for CAN
4) In all cases (also for TSD shutdown): to enable the Bus transmission again, TXD needs to be HIGH for a certain time (transmitter enable time).

WK_STAT_1

Wake-up Source and Information Status (Address 100 0110$_B$)

POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: xxxx 0xxx$_B$**

7	6	5	4	3	2	1	0
LIN2_WU	**LIN1_WU**	**CAN_WU**	**TIMER_WU**	**Reserved**	**WK3_WU**	**WK2_WU**	**WK1_WU**
rc	rc	rc	rc	r	rc	rc	rc

Field	Bits	Type	Description
LIN2_WU	7	rc	**Wake up via LIN2 Bus (GD33AP2361/GD33AP2362: Reserved)** 0_B , No Wake up 1_B , Wake up
LIN1_WU	6	rc	**Wake up via LIN1 Bus (GD33AP2361: Reserved)** 0_B , No Wake up 1_B , Wake up
CAN_WU	5	rc	**Wake up via CAN Bus** 0_B , No Wake up 1_B , Wake up
TIMER_WU	4	rc	**Wake up via TimerX** 0_B , No Wake up 1_B , Wake up
Reserved	3	r	**Reserved, always reads as 0**
WK3_WU	2	rc	**Wake up via WK3** 0_B , No Wake up 1_B , Wake up
WK2_WU	1	rc	**Wake up via WK2** 0_B , No Wake up 1_B , Wake up
WK1_WU	0	rc	**Wake up via WK1** 0_B , No Wake up 1_B , Wake up

Note: The respective wake source bit will also be set when the device is woken from SBC Fail-Safe Mode

WK_STAT_2

Wake-up Source and Information Status (Address 100 0111$_B$)

POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: 00xx 0000$_B$**

7	6	5	4	3	2	1	0
Reserved	Reserved	GPIO2_WU	GPIO1_WU	Reserved	Reserved	Reserved	Reserved
r	r	rc	rc	r	r	r	r

Field	Bits	Type	Description
Reserved	7:6	r	Reserved, always reads as 0
GPIO2_WU	5	rc	Wake up via GPIO2 0_B , No Wake up 1_B , Wake up
GPIO1_WU	4	rc	Wake up via GPIO1 0_B , No Wake up 1_B , Wake up
Reserved	3:0	r	Reserved, always reads as 0

WK_LVL_STAT

WK Input Level (Address 100 1000$_B$)

POR / Soft Reset Value: xx00 0xxx$_B$; **Restart Value: xxxx 0xxx$_B$**

7	6	5	4	3	2	1	0
SBC_DEV _LVL	CFGP	GPIO2_LVL	GPIO1_LVL	Reserved	WK3_LVL	WK2_LVL	WK1_LVL
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
SBC_DEV _LVL	7	r	Status of SBC Operating Mode at FO3/TEST Pin 0_B , User Mode activated 1_B , SBC Development Mode activated
CFGP	6	r	Device Configuration Status 0_B , No external pull-up resistor connected on INT (Config 2/4) 1_B , External pull-up resistor connected on INT (Config 1/3)
GPIO2_LVL	5	r	Status of GPIO2 (if selected as GPIO) 0_B , Low Level (=0) 1_B , High Level (=1)
GPIO1_LVL	4	r	Status of GPIO1 (if selected as GPIO) 0_B , Low Level (=0) 1_B , High Level (=1)
Reserved	3	r	Reserved, always reads as 0
WK3_LVL	2	r	Status of WK3 0_B , Low Level (=0) 1_B , High Level (=1)

WK2_LVL	1	r	**Status of WK2** 0_B , Low Level (=0) 1_B , High Level (=1)
WK1_LVL	0	r	**Status of WK1** 0_B , Low Level (=0) 1_B , High Level (=1)

Note: GPIOx_LVL is updated in SBC Normal and Stop Mode if configured as wake input, low-side switch or high-side switch.
In cyclic sense or wake mode, the registers contain the sampled level, i.e. the registers are updated after every sampling. The GPIOs are not capable of cyclic sensing.
If selected as GPIO then the respective level is shown even if configured as low-side or high-side.

HS_OC_OT_STAT
High-Side Switch Overload Status (Address 101 0100$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0000 xxxx$_B$

7	6	5	4	3	2	1	0
Reserved	**Reserved**	**Reserved**	**Reserved**	**HS4_OC_OT**	**HS3_OC_OT**	**HS2_OC_OT**	**HS1_OC_OT**
r	r	r	r	rc	rc	rc	rc

Field	Bits	Type	Description
Reserved	7:4	r	**Reserved, always reads as 0**
HS4_OC_OT	3	rc	**Overcurrent & Overtemperature Detection HS4** 0_B , No OC or OT 1_B , OC or OT detected
HS3_OC_OT	2	rc	**Overcurrent & Overtemperature Detection HS3** 0_B , No OC or OT 1_B , OC or OT detected
HS2_OC_OT	1	rc	**Overcurrent & Overtemperature Detection HS2** 0_B , No OC or OT 1_B , OC or OT detected
HS1_OC_OT	0	rc	**Overcurrent & Overtemperature Detection HS1** 0_B , No OC or OT 1_B , OC or OT detected

Note: The OC/OT bit might be set for $V_{POR,f}$< VS < 5.5V (see also **Chapter 4.2**)

HS_OL_STAT
High-Side Switch Open-Load Status (Address 101 0101$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0000 xxxx$_B$

7	6	5	4	3	2	1	0
Reserved	**Reserved**	**Reserved**	**Reserved**	**HS4_OL**	**HS3_OL**	**HS2_OL**	**HS1_OL**
r	r	r	r	rc	rc	rc	rc

Field	Bits	Type	Description
Reserved	7:4	r	**Reserved, always reads as 0**
HS4_OL	3	rc	**Open-Load Detection HS4** 0_B , No OL 1_B , OL detected
HS3_OL	2	rc	**Open-Load Detection HS3** 0_B , No OL 1_B , OL detected
HS2_OL	1	rc	**Open-Load Detection HS2** 0_B , No OL 1_B , OL detected
HS1_OL	0	rc	**Open-Load Detection HS1** 0_B , No OL 1_B , OL detected

16.6.2 Selective Wake Status Registers

SWK_STAT
Selective Wake Status (Address 111 0000$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0x00 xxxx$_B$

7	6	5	4	3	2	1	0
Reserved	**SYNC**	**Reserved**	**Reserved**	**CANSIL**	**SWK_SET**	**WUP**	**WUF**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
SYNC	6	r	**Synchronisation (at least one CAN frame without fail must have been received)** 0_B , SWK function not working or not synchronous to CAN bus 1_B , Valid CAN frame received, SWK function is synchronous to CAN bus
Reserved	5:4	r	**Reserved, always reads as 0**
CANSIL	3	r	**CAN Silent Time during SWK operation** 0_B , tsilence not exceeded 1_B , set iftsilence is exceeded.
SWK_SET	2	r	**Selective Wake Activity** 0_B , Selective Wake is not active 1_B , Selective Wake is activated
WUP	1	r	**Wake-up Pattern Detection** 0_B , No WUP 1_B , WUP detected
WUF	0	r	**SWK Wake-up Frame Detection (acc. ISO 11898-2:2016)** 0_B , No WUF 1_B , WUF detected

Note: SWK_SET is set to flag that the selective wake functionality is activated (SYSERR = 0, CFG_VAL = 1, CAN_2 = 1). The selective wake function is activated via a CAN mode change, except if CAN = '100'.

SWK_ECNT_STAT
SWK Status (Address 111 0001$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 00xx xxxx$_B$

7	6	5	4	3	2	1	0
Reserved	**Reserved**	**ECNT_5**	**ECNT_4**	**ECNT_3**	**ECNT_2**	**ECNT_1**	**ECNT_0**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
Reserved	7:6	r	**Reserved, always reads as 0**
ECNT	5:0	r	**SWK CAN Frame Error Counter** 00 0000$_B$, No Frame Error 01 1111$_B$, 31 Frame Errors have been counted 10 0000$_B$, Error counter overflow - SWK function will be disabled

Note: If a frame has been received that is valid according to ISO 11898-1 and the counter is not zero, then the counter shall be decremented. If the counter has reached a value of32, the following actions shall be performed: Selective Wake function shall be disabled,SYSERR shall be set and CAN wake capable function shall be enabled, which leads to a wake with the next WUP.

SWK_CDR_STAT1
CDR Status 1 Register (Address 111 0010$_B$)
POR Value: 1010 0000$_B$/ Soft Reset Value: yyyy yyyy$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
N_AVG_11	**N_AVG_10**	**N_AVG_9**	**N_AVG_8**	**N_AVG_7**	**N_AVG_6**	**N_AVG_5**	**N_AVG_4**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
NAVG_SAT	7:0	r	**Output Value from Filter Block** N_AVG is representing the integer part of the number of selected input clock frequency per CAN bus bit. N_AVG[11:4] e.g.160.75

SWK_CDR_STAT2
CDR Status 2 Register (Address 111 0011$_B$)
POR Value: 0000 0000$_B$ / Soft Reset Value: yyyy yyyy$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
N_AVG_3	**N_AVG_2**	**N_AVG_1**	**N_AVG_0**	**reserved**	**reserved**	**reserved**	**reserved**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
NAVG_SAT	7:4	r	**Output Value from Filter Block** N_AVG is representing the fractional part of the number of selected input clock frequency per CAN bus bit. N_AVG[3:0] e.g.160.75
Reserved	3:0	r	**Reserved, always reads as 0**

16.6.3 Family and Product Information Register

FAM_PROD_STAT
Family and Product Identification Register (Address 111 1110$_B$)
POR / Soft Reset Value: 1011 yyyy $_B$; Restart Value: 1011 yyyy$_B$

7	6	5	4	3	2	1	0
FAM_3	**FAM_2**	**FAM_1**	**FAM_0**	**PROD_3**	**PROD_2**	**PROD_1**	**PROD_0**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
FAM	7:4	r	**SBC Family Identifier (bit4=LSB; bit7=MSB)** 1001$_B$, Basic SBC Family 1011$_B$, Mid SBC Family xxxx$_B$, reserved for future products
PROD	3:0	r	**SBC Product Identifier (bit0=LSB; bit3=MSB)** 0001$_B$, GD33AP2363QV (VCC1=5V, 2 LIN, no SWK) 0010$_B$, GD33AP2363-3QV (VCC1 = 5V, 2 LIN, with SWK) 0011$_B$, GD33AP2363QVV33 (VCC1 = 3.3V, 2 LIN, no SWK) 0100$_B$, GD33AP2363-3QVV33 (VCC1 = 3.3V, 2 LIN, with SWK) 0101$_B$, GD33AP2362QV (VCC1=5V, 1 LIN, no SWK) 0110$_B$, GD33AP2362-3QV (VCC1 = 5V, 1 LIN, with SWK) 0111$_B$, GD33AP2362QVV33 (VCC1 = 3.3V, 1 LIN, no SWK) 1000$_B$, GD33AP2362-3QVV33 (VCC1 = 3.3V, 1 LIN, with SWK) 1001$_B$, GD33AP2361QV (VCC1=5V, 0 LIN, no SWK) 1010$_B$, GD33AP2361-3QV (VCC1 = 5V, 0 LIN, with SWK) 1011$_B$, GD33AP2361QVV33 (VCC1 = 3.3V, 0 LIN, no SWK) 1100$_B$, GD33AP2361-3QVV33 (VCC1 = 3.3V, 0 LIN, with SWK)

Notes

1. The actual default register value after POR, Soft Reset or Restart of PROD will depend on the respective product. Therefore the value ‘y’ is specified.
2. SWK = Selective Wake feature in CAN Partial Networking standard

16.7 Electrical Characteristics

Table 39 Electrical Characteristics

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			
SPI frequency							
Maximum SPI frequency	$f_{SPI,max}$	–	–	4.0	MHz	1)	
SPI Interface; Logic Inputs SDI, CLK and CSN							
H-input Voltage Threshold	V_{IH}	–	–	0.7* V_{CC1}	V	–	
L-input Voltage Threshold	V_{IL}	0.3* V_{CC1}	–	–	V	–	
Hysteresis of input Voltage	V_{IHY}	0.08 × V_{CC1}	0.12 × V_{CC1}	0.5 × V_{CC1}	V	1)	
Pull-up Resistance at pin CSN	R_{ICSN}	20	40	80	kΩ	V_{CSN} = 0.7 x V_{CC1}	
Pull-down Resistance at pin SDI and CLK	$R_{ICLK/SDI}$	20	40	80	kΩ	$V_{SDI/CLK}$ = 0.2 x V_{CC1}	
Input Capacitance at pin CSN, SDI or CLK	C_I	–	10	–	pF	1)	
Logic Output SDO							
H-output Voltage Level	V_{SDOH}	V_{CC1} - 0.4	V_{CC1} - 0.2	–	V	I_{DOH} = -1.6 mA	
L-output Voltage Level	V_{SDOL}	–	0.2	0.4	V	I_{DOL} = 1.6 mA	
Tristate Leakage Current	I_{SDOLK}	-10	–	10	µA	V_{CSN} = V_{CC1}; 0 V < V_{DO} < V_{CC1}	
Tristate Input Capacitance	C_{SDO}	–	10	15	pF	1)	
Data Input Timing[1)]							
Clock Period	t_{pCLK}	250	–	–	ns	–	
Clock High Time	t_{CLKH}	125	–	–	ns	–	
Clock Low Time	t_{CLKL}	125	–	–	ns	–	
Clock Low before CSN Low	t_{bef}	125	–	–	ns	–	
CSN Setup Time	t_{lead}	250	–	–	ns	–	
CLK Setup Time	t_{lag}	250	–	–	ns	–	
Clock Low after CSN High	t_{beh}	125	–	–	ns	–	
SDI Set-up Time	t_{DISU}	100	–	–	ns	–	
SDI Hold Time	t_{DIHO}	50	–	–	ns	–	
Input Signal Rise Time at pin SDI, CLK and CSN	t_{rIN}	–	–	50	ns	–	

Table 39 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Note
		Min.	Typ.	Max.			
Input Signal Fall Time at pin SDI, CLK and CSN	t_{fIN}	–	–	50	ns	–	
Delay Time for Mode Changes[2)]	$t_{Del,Mode}$	–	–	6	µs	includes internal oscillator tolerance	
CSN High Time	$t_{CSN(high)}$	3	–	–	µs	–	
Data Output Timing[1)]							
SDO Rise Time	t_{rSDO}	–	30	80	ns	C_L = 100 pF	
SDO Fall Time	t_{fSDO}	–	30	80	ns	C_L = 100 pF	
SDO Enable Time	t_{ENSDO}	–	–	50	ns	low impedance	
SDO Disable Time	t_{DISSDO}	–	–	50	ns	high impedance	
SDO Valid Time	t_{VASDO}	–	–	50	ns	C_L = 100 pF	

1) Not subject to production test; specified by design

2) Applies to all mode changes triggered via SPI commands

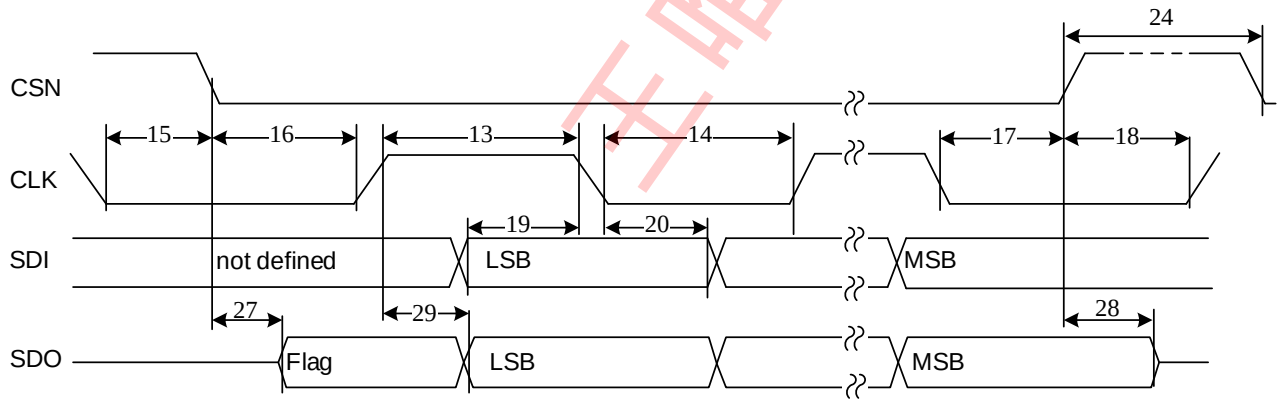


Figure 63 SPI Timing Diagram

Note: Numbers in drawing correlate to the last 2 digits of the Number field in the Electrical Characteristics table.

17 Application Information

17.1 Application Diagram

Note: For GD33AP2362 LIN2/TXDLIN2/RXDLIN2 shall be left open.
For GD33AP2361 LIN1/TXDLIN1/RXDLIN1/LIN2/TXDLIN2/RXDLIN2 shall be left open.

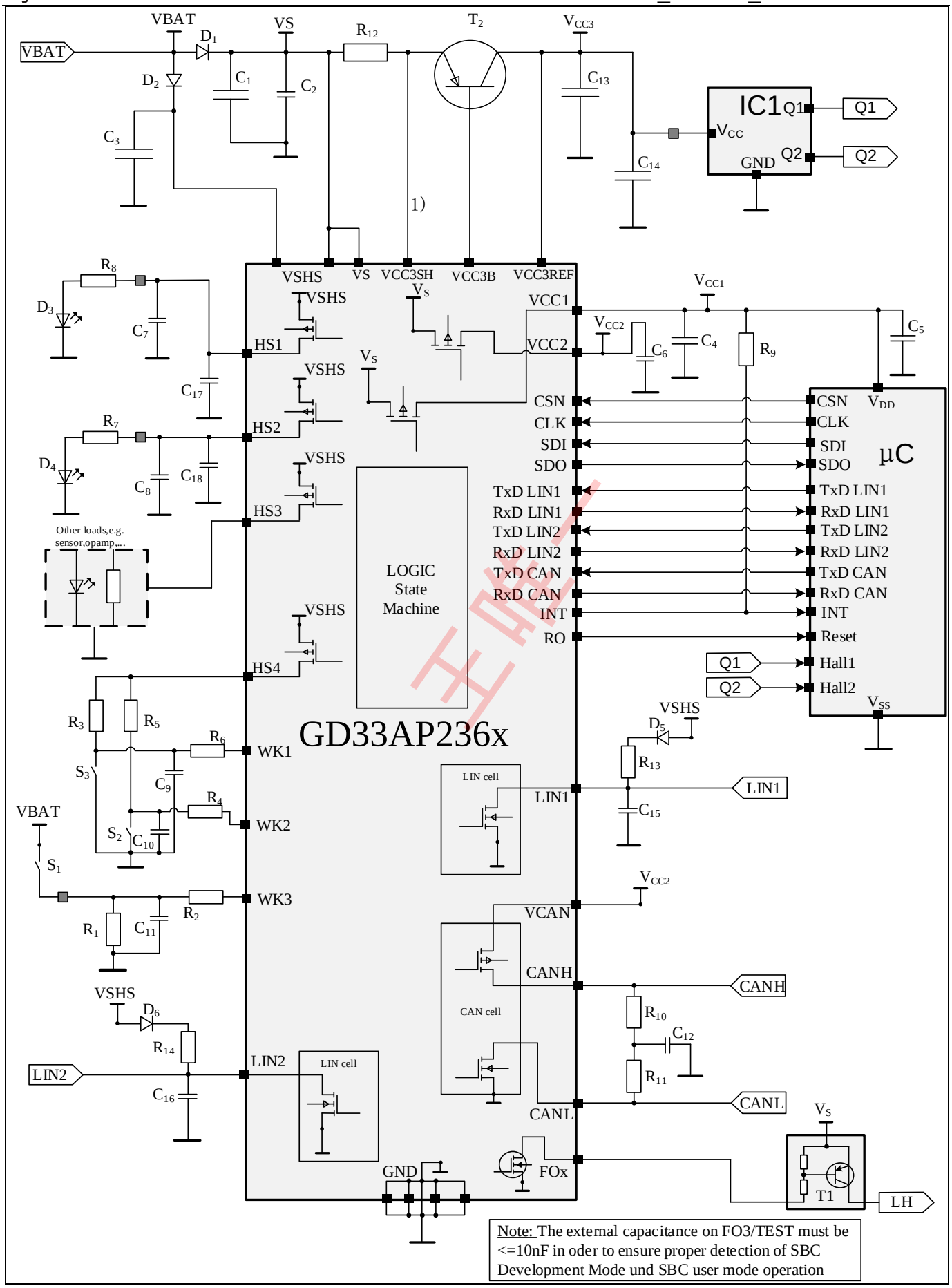


Figure 64 Simplified Application Diagram

1) It is highly recommended to add a typ. 200Ω series resistor at the pin VCC3SH (if VCC3 is used) to prevent any damage of the SBC in case a short failure of the external PNP (T2) occurs.

Note: Unused outputs are recommended to be left unconnected on the application board. If unused output pins are routed to an external connector which leaves the ECU, then these pins should have provision for a zero ohm jumper (depopulated if unused) or ESD protection.

Table 40 Bill of Material for Simplified Application Diagram

Ref.	Typical Value	Purpose / Comment
Capacitances		
C1	68µF	Buffering capacitor to cut off battery spikes, depending on application
C2	100nF	EMC, blocking capacitor
C3	22µF	Buffering capacitor to cutoff battery spikes from VSHS as separate supply input; Depending on application, only needed if VSHS is not connected to VS;
C4	2.2µF low ESR	As required by application, min. 470nF for stability and max. 68µF recommended
C5	100nF ceramic	Spike filtering, improve stability of supply for microcontroller; not needed for SBC
C6	2.2µF low ESR	Blocking capacitor, min. 470nF for stability; if used for CAN supply place a 100nF ceramic capacitor in addition very close to VCAN pin for optimum EMC behavior
C7	33nF	As required by application, mandatory protection for off-board connections
C8	33nF	As required by application, mandatory protection for off-board connections
C17	47pF	Only required in case of off-board connection to optimize EMC behavior, place close to pin
C18	47pF	Only required in case of off-board connection to optimize EMC behavior, place close to pin
C9	10nF	Spike filtering, as required by application, mandatory protection for off-board connections (see also Simplified Application Diagram with the Alternate Measurement Function)
C10	10nF	Spike filtering, as required by application, mandatory protection for off-board connections
C11	10nF	Spike filtering, as required by application, mandatory protection for off-board connections
C12	4.7nF / OEM dependent	Split termination stability
C13	10µFlow ESR	Stability of VCC3, ceramic capacitor, e.g. Murata 10 µF/10 V GCM31CR71A106K64L or 2x 4.7 µF/10 V
C14	47nF	Only required in case of off-board connection to optimize EMC behavior, place close to connector
C15	1nF / OEM dependent	LIN master termination
C16	1nF / OEM dependent	LIN master termination
Resistances		
R1	10kΩ	Wetting current of the switch, as required by application

Table 40 Bill of Material for Simplified Application Diagram (cont'd)

Ref.	Typical Value	Purpose / Comment
R2	10kΩ	Limit the WK pin current,e.g. for ISO pulses
R3	10kΩ	Wetting current of the switch,as required by application
R4	10kΩ	Limit the WK pin current,e.g. for ISO pulses
R5	10kΩ	Wetting current of the switch,as required by application
R6	10kΩ	Limit the WK pin current, e.g. for ISO pulses
R7	depending on LED config.	LED current limitation, as required by application
R8	depending on LED config.	LED current limitation, as required by application
R9	47pF	Selection of hardware configuration 1/3，i.e. in case of WD failure SBC Restart Mode is entered. If not connected, then hardware configuration 2/4 is selected
R10	60Ω / OEM dependent	CAN bus termination
R11	60Ω / OEM dependent	CAN bus termination
R12	1Ω shunt, depending on required current limitation or load sharing ratio	Sense shunt for ICC3 current limitation (configured to typ. 235mA with 1Ω shunt) for stand-alone configuration; Setting of load sharing ratio (here ICC3/ICC1 = 1) in load sharing configuration.
R13	1kΩ / OEM dependent	LIN master termination (if configured as a LIN master)
R14	1kΩ / OEM dependent	LIN master termination (if configured as a LIN master)
R15	10kΩ	WK1 pin current limitation, e.g. for ISO pulses, for alternate measurement function (see also Simplified Application Diagram with the Alternate Measurement Function)
R16	depending on application and microcontroller	Voltage Divider resistor to adjust measurement voltage to microcontroller ADC input range (see also Simplified Application Diagram with the Alternate Measurement Function)
R17	depending on application and microcontroller	Voltage Divider resistor to adjust measurement voltage to microcontroller ADC input range (see also Simplified Application Diagram with the Alternate Measurement Function)
Active Components		
D1	e.g. BAS 3010A	Reverse polarity protection for VS supply pins
D2	e.g. BAS 3010A	Reverse polarity protection for VSHS supply pin；if separate supplies are not needed，then connect VSHS to VS pins
D3	LED	As required by application，configure series resistor accordingly
D4	LED	As required by application，configure series resistor accordingly
D5	e.g. BAS70	Requested by LIN standard；reverse polarity protection of network
D6	e.g. BAS70	Requested by LIN standard；reverse polarity protection of network
T1	e.g. BCR191W	High active FO control
T2	BCP 52-16，	Power element of VCC3，current limit or load sharing ratio to be configured via shunt
	MJD 253， ON Semi	Alternative power element of VCC3
µC	e.g. TC2xxx	Microcontroller

Note: This is a simplified example of an application circuit. The function must be verified in the real application.

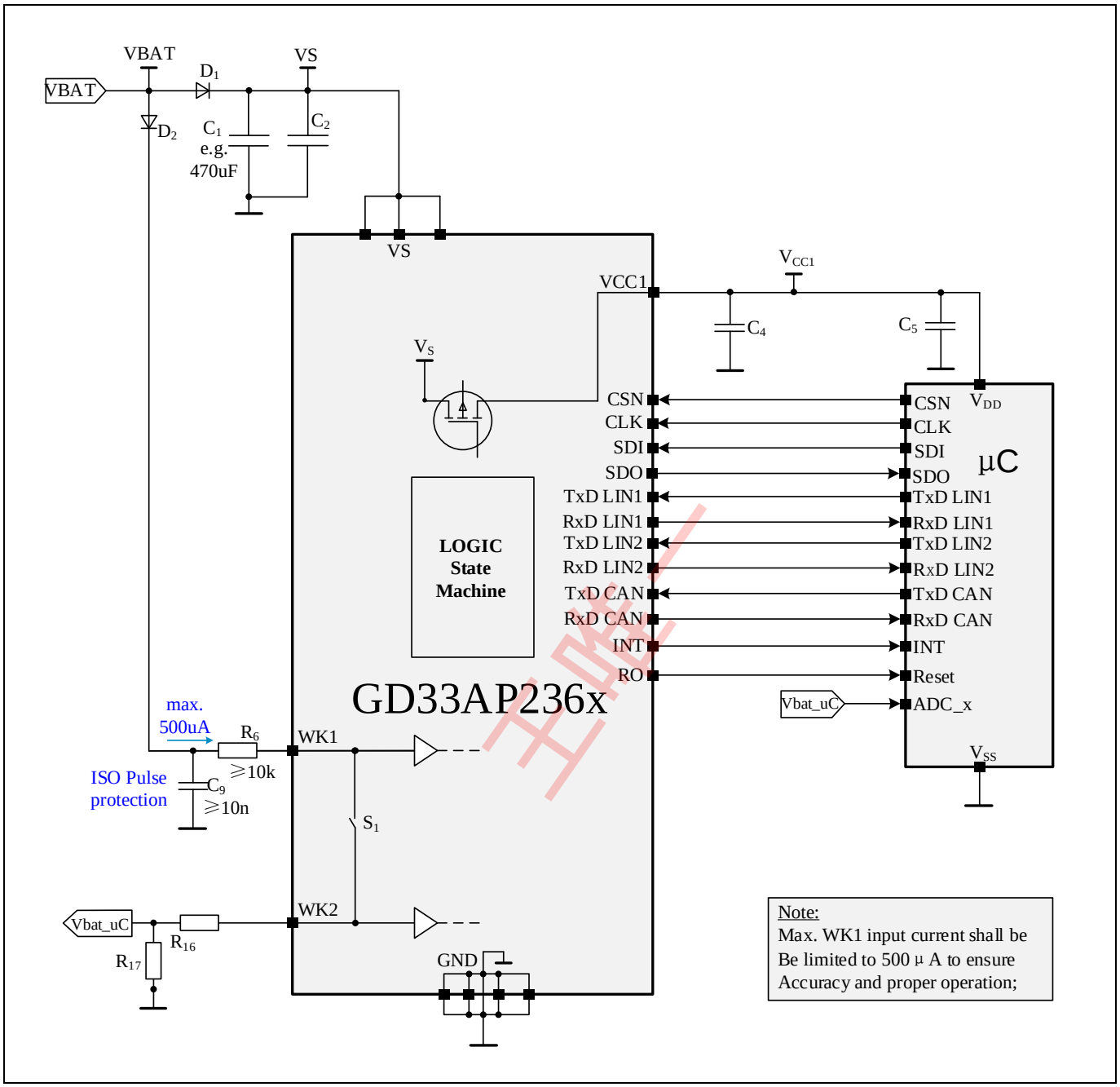


Figure 65 Simplified Application Diagram with the Alternate Measurement Function via WK1 and WK2

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.WK1 must be connected to signal to be measured and WK2 is the output to the microcontroller supervision function. The maximum current into WK1 must be <500uA. The minimum current into WK1 should be >5uA to ensure proper operation. For GD33AP2362 LIN2/TXDLIN2/RXDLIN2 shall be left open. For GD33AP2361 LIN1/TXDLIN1/RXDLIN1/LIN2/TXDLIN2/RXDLIN2 shall be left open.

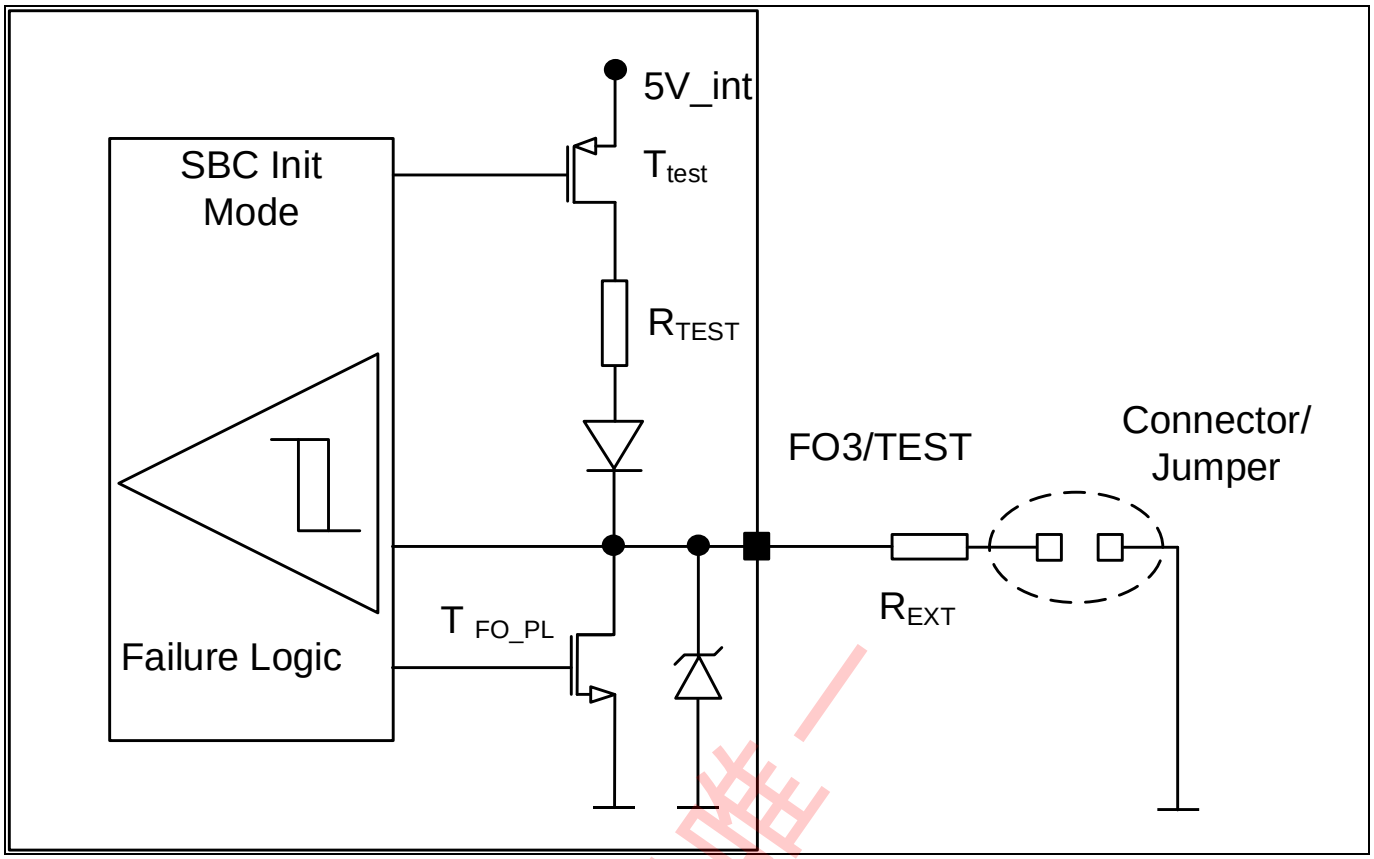
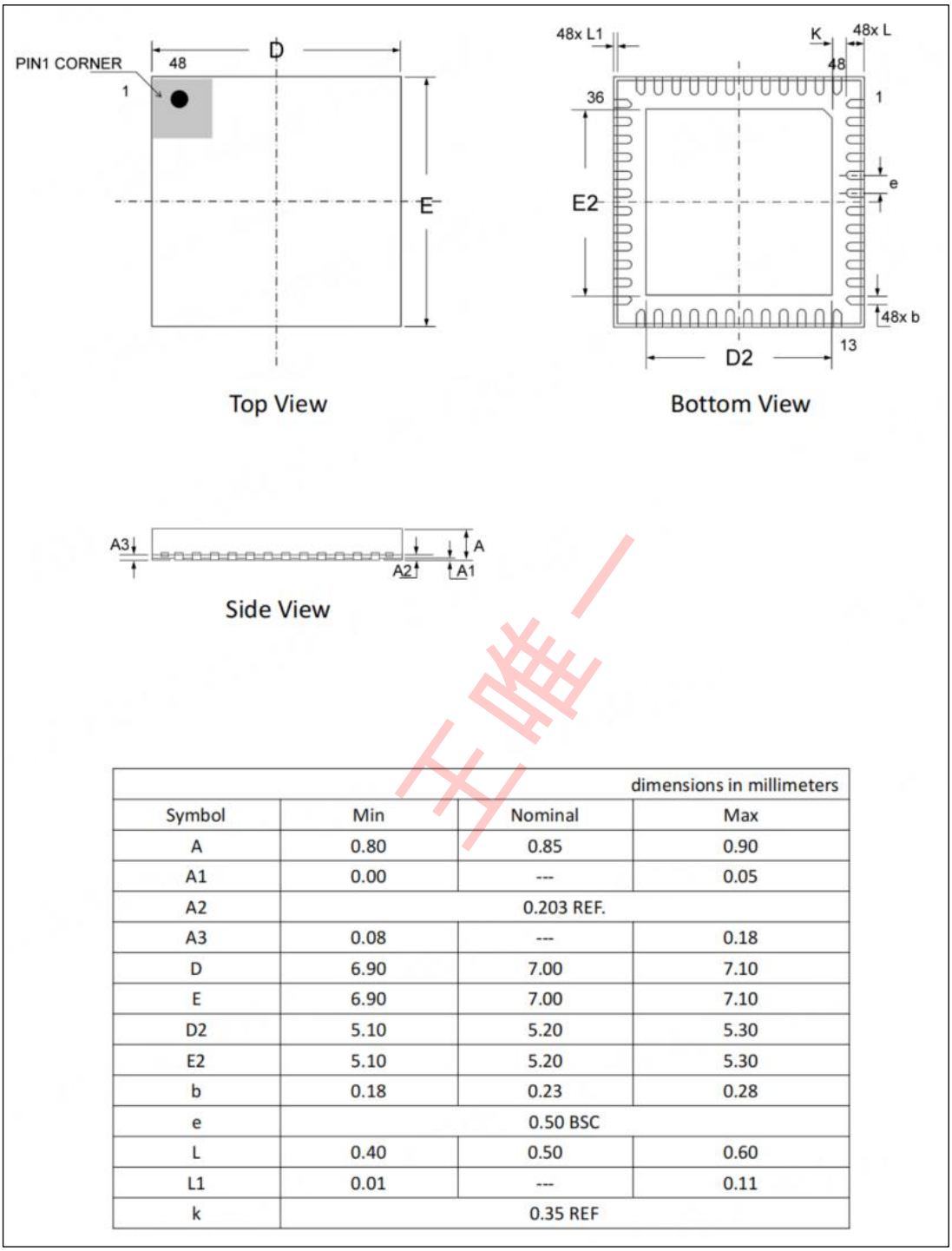


Figure 66 Hint for Increasing the Robustness of pinFO3/TEST during Debugging or Programming

18 Package Outlines



dimensions in millimeters			
Symbol	Min	Nominal	Max
A	0.80	0.85	0.90
A1	0.00	---	0.05
A2		0.203 REF.	
A3	0.08	---	0.18
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D2	5.10	5.20	5.30
E2	5.10	5.20	5.30
b	0.18	0.23	0.28
e		0.50 BSC	
L	0.40	0.50	0.60
L1	0.01	---	0.11
k		0.35 REF	

Figure 69 VQFN-48 Package Information

19 Revision History

Revision	Date	Changes
V1.0	2026/3	Released Version V1.0.