GD24CL256B

DATASHEET

Contents

1 FEATURES

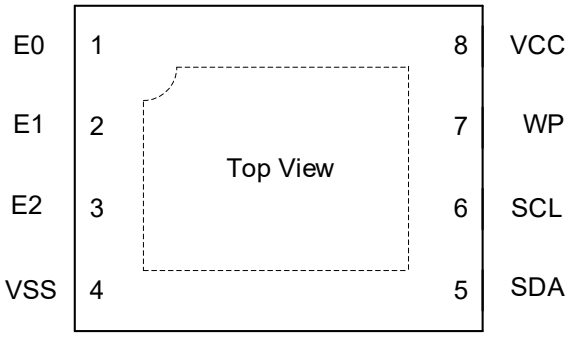
- Compatible with following I²C bus modes
  - 1 MHz
  - 400 KHz
  - 100 KHz
- Memory array
  - 256K bit (32K Byte) of EEPROM
  - Page size: 64 Byte
  - Additional write lockable security page
- Random and sequential read modes
- Write protect of the whole memory array
- On−Chip ECC
  - 1-bit correction every 4-Byte
- Endurance and Data Retention
  - More than 4 million write cycles
  - More than 200-years data retention
- Write
  - Byte write within 5 ms
  - Page write within 5 ms
- Single supply voltage
  - 1.7-5.5V
- Operating temperature range
  - from -40℃ up to +85℃
- Package Information
  - UDFN8 (2x3mm)
  - SOP8 150mil
  - SOT23-5
  - MSOP8 120mil
  - TSSOP8 173mil
  - PDIP8 300mil

2 GENERAL DESCRIPTIONS

The GD24CL256B (256K bit) electrically erasable programmable read only memory (EEPROM) supports the industrial standard 2 wire interface (I²C): Serial Clock (SCL), Serial Data (SDA). The GD24CL256B contains a memory array of 256K bit (32K Byte), which is organized in 64 Byte per page. The device operates with 1 MHz (or less) clock frequency.

CONNECTION DIAGRAM AND PIN DESCRIPTION

Figure 1 Connection Diagram for UDFN8 package



8 - LEAD UDFN

Table 1. Pin Description for UDFN8 Package

Pin No.	Pin Name	I/O	Description
1	E0	I	Chip enable Input
2	E1	I	Chip enable Input
3	E2	I	Chip enable Input
4	VSS		Ground
5	SDA	I/O	Data Input / Output
6	SCL	I	Serial Clock Input
7	WP	I	Write Protect, Low Enable Write
8	VCC		Power Supply

Note:

1. The exposed pad on this package can be connected to VSS or left floating.
2. If the E0, E1, E2 or WP pins are not driven, they are internally pulled down to VSS. It is recommended to connect these pins to a known state whenever possible.

Figure 2 Connection Diagram for SOT23-5 package

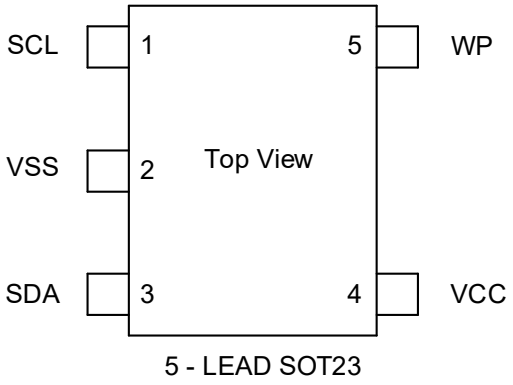


Table 2. Pin Description for SOT23-5 Package

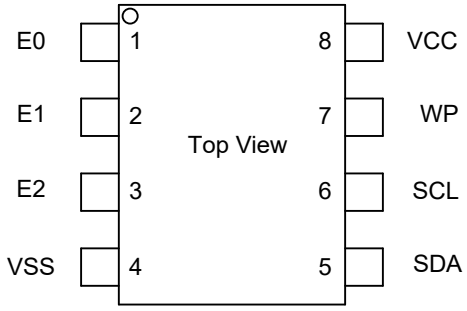
Pin No.	Pin Name	I/O	Description
1	SCL	I	Serial Clock Input
2	VSS		Ground
3	SDA	I/O	Data Input / Output
4	VCC		Power Supply
5	WP	I	Write Protect, Low Enable Write

Note:

1. If the WP pins are not driven, it is internally pulled down to VSS. It is recommended to connect these pins to a known state whenever possible.

2. For the SOT23-5 package, Chip enable inputs are not available. During device addressing, the E0, E1, E2 Chip enable address bits should be set to 0.

Figure 3 Connection Diagram for SOP8/MSOP8/TSSOP8/PDIP8 package



8 - LEAD SOP/MSOP/TSSOP/PDIP

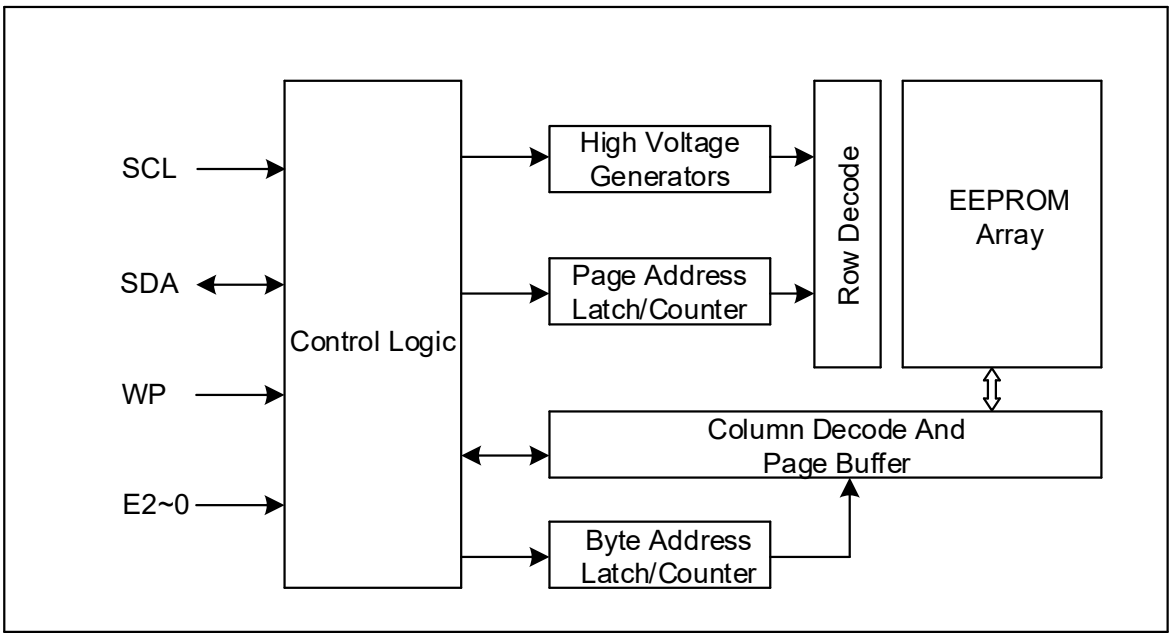
Table 3. Pin Description for SOP8/MSOP8/TSSOP8/PDIP8 Package

Pin No.	Pin Name	I/O	Description
1	E0	I	Chip enable Input
2	E1	I	Chip enable Input
3	E2	I	Chip enable Input
4	VSS		Ground
5	SDA	I/O	Data Input / Output
6	SCL	I	Serial Clock Input
7	WP	I	Write Protect, Low Enable Write
8	VCC		Power Supply

Note:

1. If the E0, E1, E2 or WP pins are not driven, they are internally pulled down to VSS. It is recommended to connect these pins to a known state whenever possible.

BLOCK DIAGRAM



3 PIN DESCRIPTIONS

SCL

The SCL (Serial Clock) is used to receive the clock signal from the master, while the bidirectional SDA is used to receive command and data information from the master as well as to send data back to the master. Data is latched into the device on the rising edge of SCL and output from the device on the falling edge of SCL.

SDA

The SDA (Serial Data) is a bidirectional input/output pin used to transfer data in or data out of the device. The SDA pin is an open drain that may be wired-AND with other open drain or open collector signals on the same bus. The SDA pin must be pulled high using an external pull-up resistor.

E2, E1, E0

The E2, E1 and E0 (Chip Enable) pins are device address inputs. These inputs must be tied to VCC or VSS. Typically, the E2, E1, and E0 pins are for hardware addressing and a total of 8 devices can be connected on a single bus system. If these pins are left floating, the E2, E1, and E0 pins will be internally pulled down to VSS.

WP

The WP (Write Protect) pin is write-protect input, when the WP pin is connected to VCC, the entire memory array is protected. When the WP pin is connected to VSS, the normal write operations are allowed. If the WP pin is left floating, the WP pin will be internally pulled down to VSS. However, it is recommended to connect the WP pin to a known state whenever possible.

VCC

The VCC (Supply Voltage) must be stable within 1.7V(min) ~ 5.5V(max) before selecting the device and issuing instructions to it. In order to secure a stable DC supply voltage, it is recommended to decouple the VCC line with a suitable capacitor close to the VCC/VSS pins.

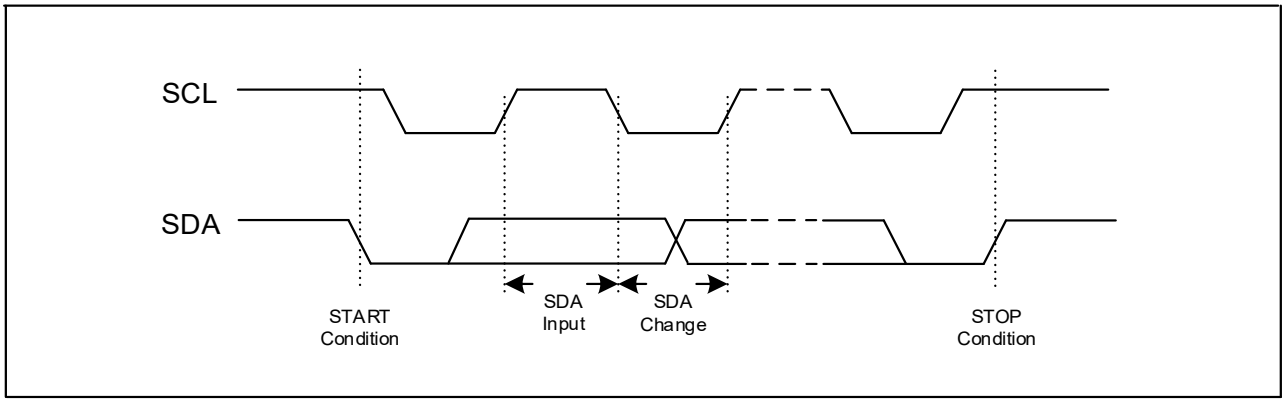
This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle (tw).

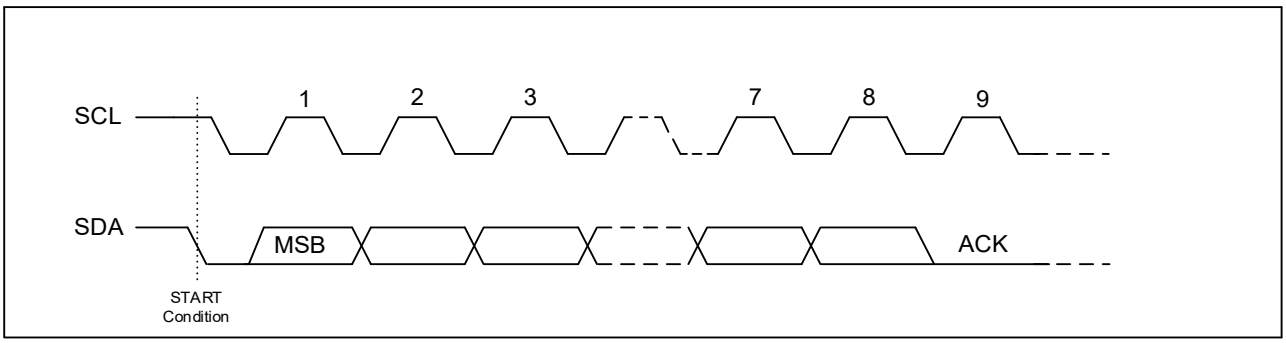
4 DEVICE OPERATIONS

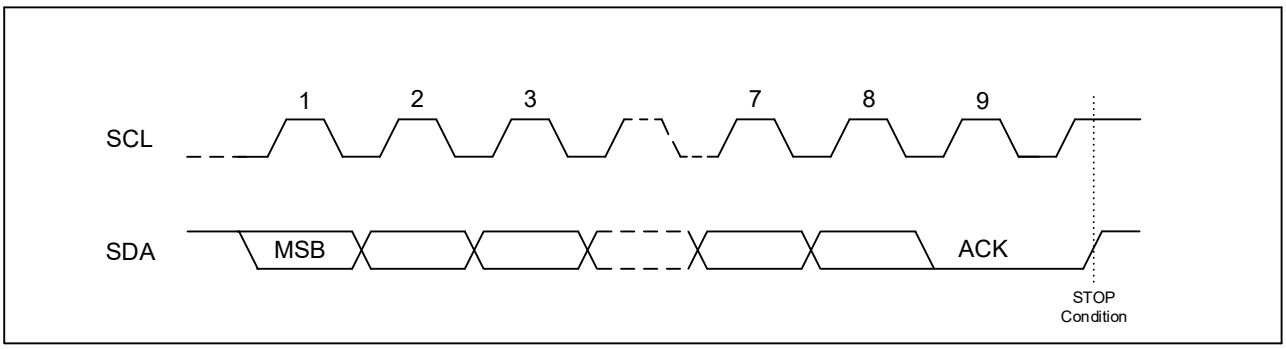
The device uses a simple I²C-compatible two-wire digital serial interface to communicate with a master. The master initiates and controls all read and write operations to the devices on the serial bus, and both the master and the devices can transmit and receive data on the bus.

The serial interface is comprised of SCL (Serial Clock) and SDA (Serial Data). The SCL is used to receive the clock signal from the master, while the bidirectional SDA is used to receive command and data information from the master as well as to send data back to the master. Data is latched into the device on the rising edge of SCL and output from the device on the falling edge of SCL.

Figure 4. I²C bust protocol







4.1 Start Condition

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command. The master uses a Start condition to initiate any data transfer sequence.

4.2 Stop Condition

A low-to-high transition of SDA with SCL high is a stop condition which terminates communication between the device and the master. All commands must end with a stop condition.

4.3 Data Transition

During a data transfer, the SDA must be stable during the rising edge of SCL, data on the SDA may change only during SCL low time periods. Data changes during SCL high periods will indicate a Start or Stop condition.

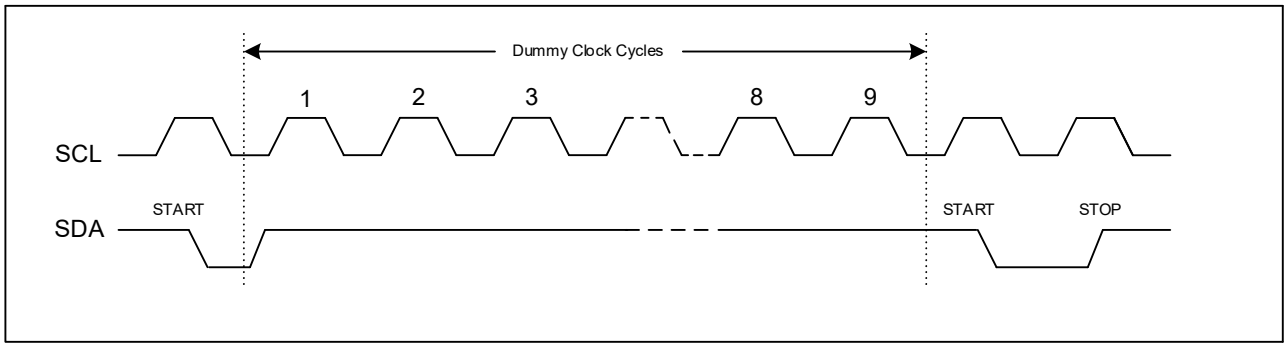
4.4 Acknowledge

After a Byte of data is received, the receiving device is required to generate an ACK. During the 9th clock pulse period, the receiving device pulls down the SDA to acknowledge the receipt of the Byte of data.

4.5 Software Reset

Software reset is executed to avoid malfunction after power loss or system reset or interruption in protocol. Software reset steps: start condition -> clock nine dummy cycles -> start condition followed by stop condition, as shown below. The device is ready for the next communication after the above steps have been completed.

Figure 5. Software reset



4.6 ECC Function

Error Correction Codes (ECC) is a commonly used technique to improve device reliability. The ECC logic is implemented on each group of 4 Bytes data (A[1:0] = 0, 0). If a single bit out of the 4 Bytes happens to be erroneous during a read operation, the ECC detects this bit and replaces it with the correct value.

Even if the ECC function is performed on groups of 4 Bytes, a single Byte can be written/cycled independently. In this case, the ECC function also writes/cycles the three other Bytes located in the same group.

The maximum cycling value is defined at group level and the cycling can be distributed over the 4 Bytes of the group. The sum of cycles of each Byte in the same group must remain below the maximum value.

4.7 Device Addressing

To access the device, the master must initiate a Start condition. Following this, the master sends the 4-bit Device type identifier and 3-bit Chip enable address E2, E1 and E0, shown in Table 4 (most significant bit first). For the SOT23-5 package, the Chip enable address pins are not available, the E0, E1, E2 Chip enable address bits should be set to 0.

The eighth bit (bit 0) of the device address Byte is the Read/Write (R/$\overline{W}$) Select bit. R/$\overline{W}$ bit is set to 1 for read and 0 for write operations.

If a match occurs on the device address Byte, the device will return an Acknowledge (ACK). If the device does not match the device address Byte, the device will not return ACK.

After sending the device address, the master needs to send the Byte address as specified in Table 5, Table 6.

Table 4. Device address

	Device type identifier				Chip enable address			R/$\overline{W}$
	Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Memory array	1	0	1	0	E2	E1	E0	R/$\overline{W}$
Security Page	1	0	1	1	E2	E1	E0	R/$\overline{W}$

Table 5. First Byte address

	Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Memory array	X	A14	A13	A12	A11	A10	A9	A8
Security Page	X	X	X	X	X	0	X	X

Table 6. Second Byte address

	Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Memory array	A7	A6	A5	A4	A3	A2	A1	A0
Security Page	X	X	A5	A4	A3	A2	A1	A0

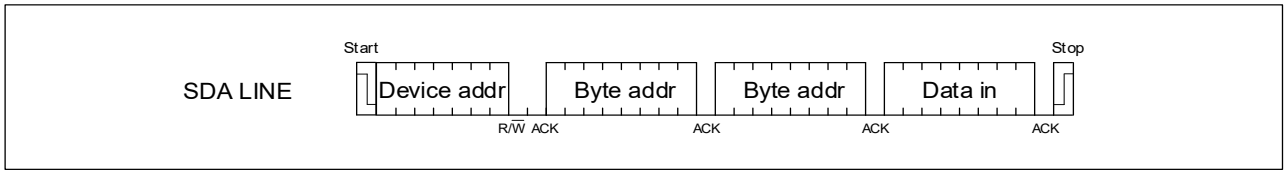
5 INSTRUCTIONS

5.1 Byte Write

The Byte Write operation is for writing the memory. The Master sends the Start condition and the device address (R/$\overline{W}$ is set to “0”) to the Slave device. After the Slave generates an ACK, the Master sends the address Byte and data Byte, the Slave generates ACK after receiving each Byte. After the Master sends the Stop condition, the self-timed program cycle (whose duration is tw) is initiated. While the program cycle is in progress, the device will not respond to any request from the Master device.

If the entire memory is protected by WP (tied to VCC), the Slave replies with NoACK. The Byte Write is not executed and the location is not modified.

Figure 6. Byte Write



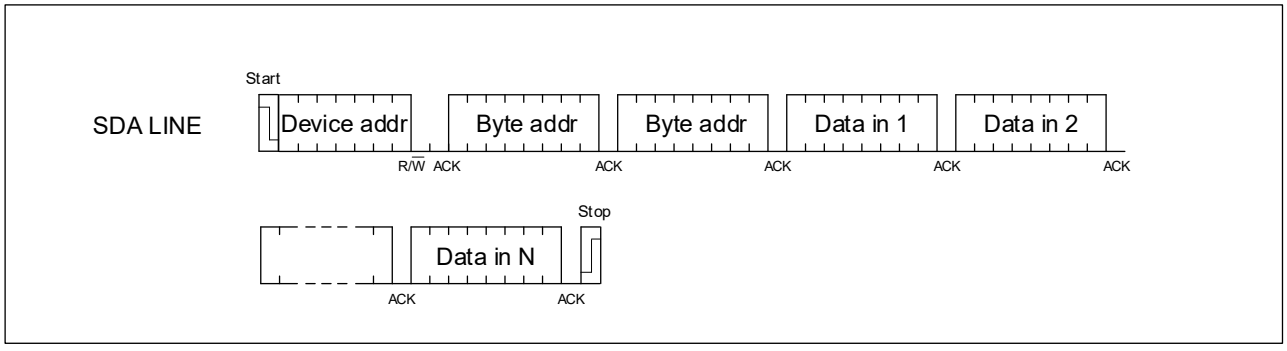
5.2 Page Write

The Page Write operation is same with Byte Write operation, but with more than one Byte data. If more Bytes are sent than will fill up to the end of the page, a roll-over occurs, the Bytes exceeding the page end are written on the same page, from location 0.

The Master sends the Start condition and the device address (R/$\overline{W}$ is set to “0”) to the Slave device. After the Slave generates an ACK, the Master sends the address Byte and data Byte, the Slave generates ACK after receiving each Byte. After the Master sends the Stop condition, the self-timed program cycle (whose duration is tw) is initiated. While the program cycle is in progress, the device will not respond to any request from the Master device.

If the entire memory is protected by WP (tied to VCC), the Slave replies with NoACK. The Page Write is not executed and the location is not modified.

Figure 7. Page Write



5.3 Current Address Read

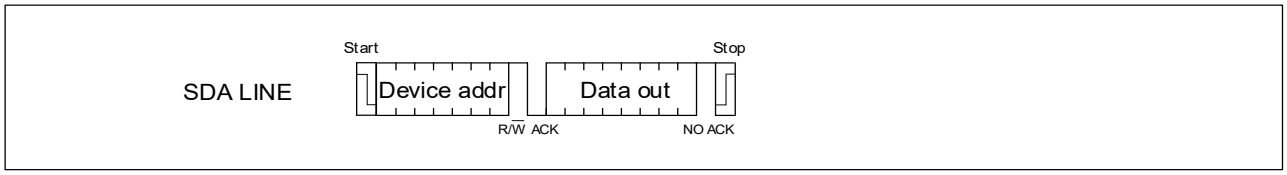
The internal address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained.

The Master sends the Start condition and the device address (R/$\overline{W}$ is set to “1”) to the Slave device. The Slave generates

an ACK and outputs the Byte addressed by the internal address counter. The master must not acknowledge the Byte, and terminates the transfer with a stop condition.

When accessing the Security Page, the address rollover during a read is from the last Byte of the Security Page to the first Byte of the Security Page. When accessing the memory, the address rollover during a read is from the last Byte of the last page to the first Byte of the first page of the memory.

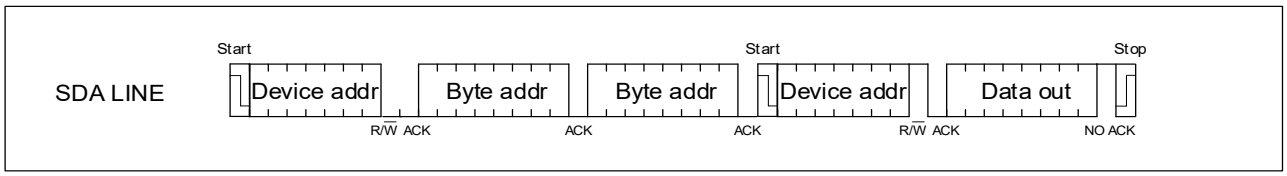
Figure 8. Current Address Read



5.4 Random Address Read

A Random Read requires a “dummy” Byte write sequence to load in the address Byte. Once the device address and address Byte are clocked in and acknowledged by the slave, the master must generate another start condition, and repeats the device address with the R/$\overline{W}$ bit set to 1. The slave acknowledges this, and outputs the contents of the addressed Byte. The master must not acknowledge the Byte, and terminates the transfer with a stop condition.

Figure 9. Random Address Read



5.5 Sequential Address Read

Sequential Address Read is initiated by either a Current Address Read or a Random Address Read. After the master receives a data Byte, it responds with acknowledge. As long as the slave receives acknowledge, it will continue to increment the Byte address and continues to output data Byte.

When the last memory address is reached, the Byte address rollover and the Sequential Address Read continues. The Sequential Address Read is terminated when the master does not acknowledge the Byte and generates a stop condition.

Figure 10. Sequential Current Read

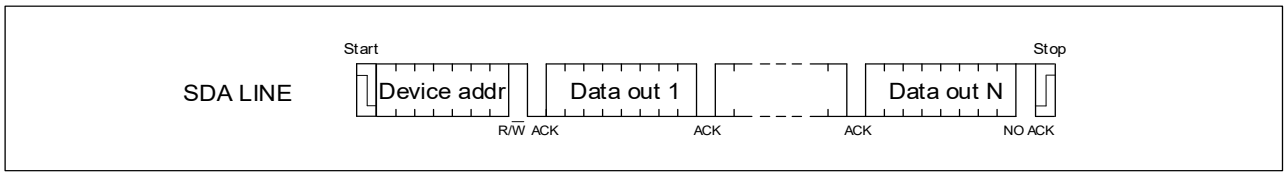
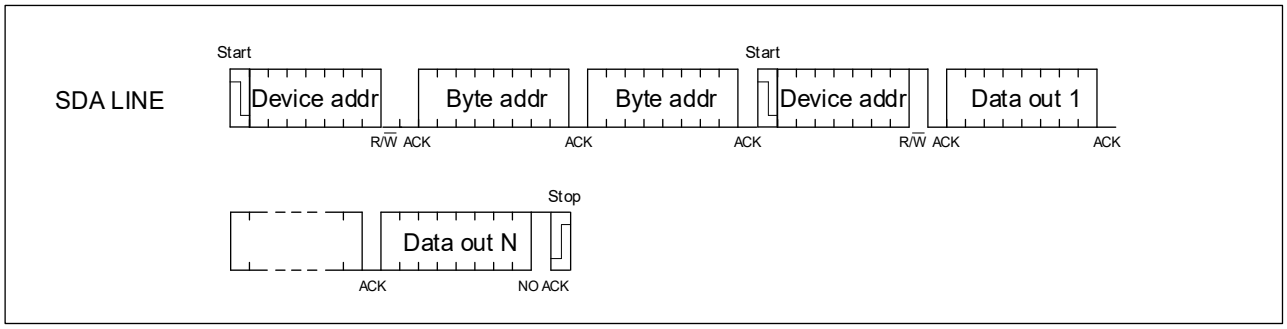


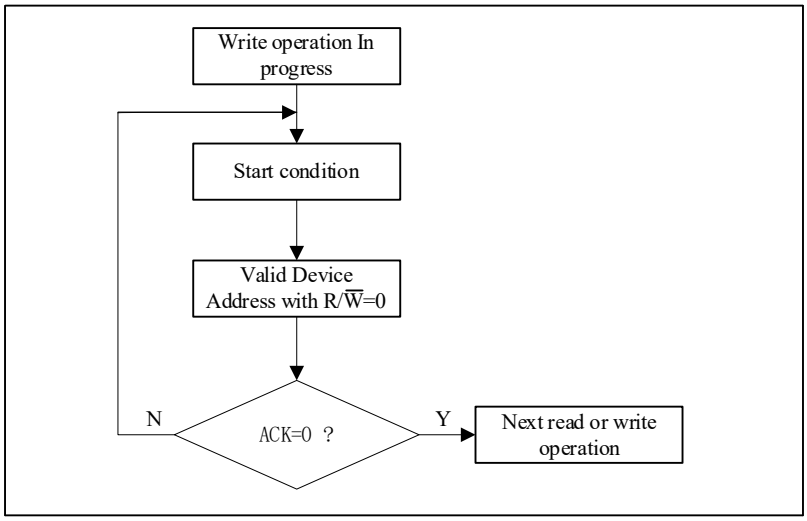
Figure 11. Sequential Random Read



5.6 Acknowledge (ACK) Polling

The tw is the maximum write time, but the typical write time is shorter. Acknowledge Polling can be implemented to check whether the write operation has ended; Acknowledge Polling is a start condition followed by the device address (R/$\overline{W}$ is set to “0”). If the write operation is in progress, no ACK is returned. If the Write operation is completed, an ACK will be returned and the host can then send the next Read or write operation. The sequence is below;

Figure 12. Acknowledge (ACK) Polling



5.7 Write Security Page

The Security Page (64 Byte) is a Page which can be written and later permanently locked in Read-only mode. It is written by the Write Security Page instruction. This instruction uses the same protocol and format as Page Write, except for the following differences:

- Device type identifier = 1011b
- MSB address bits A15~A6 are don't care except for address bit A10 which must be ‘0’. LSB address bits A5~A0 define the Byte address inside the Security page.

If the Security page is locked, the data Bytes transferred during the write security page instruction are not acknowledged (NoACK).

5.8 Lock Security Page

The lock Security page instruction permanently locks the Security page in read-only mode. The lock Security page instruction is similar to Byte write with the following specific conditions:

- Device type identifier = 1011b
- Address bit A10 must be '1'; all other address bits are don't care
- The data Byte must be equal to the binary value xxxx xx1x, where x is don't care

5.9 Read Security Page

The Security page (64 Byte) is a Page which can be written and later permanently locked in Read-only mode. The Security page can be read by issuing a read Security page instruction. This instruction uses the same protocol and format as the random address read with Device type identifier defined as 1011b. The MSB address bits A15~A6 are don't care, the LSB address bits A5~A0 define the Byte address inside the identification page. The internal Byte address is automatically incremented to the next Byte address after each Byte of data is clocked out. When the last Byte (3FH) is reached, it will roll over to 00H, the first Byte of the Security page, and continue to increment.

5.10 Read Lock Status

The locked/unlocked status of the Security page can be checked by transmitting a specific truncated command [Security Page Write instruction + one data Byte] to the device. The device returns an acknowledge bit if the Security page is unlocked, otherwise a NoACK bit if the Security page is locked.

Right after this, it is recommended to transmit to the device a start condition followed by a stop condition, so that:

- Start: the truncated command is not executed because the start condition resets the device internal logic,
- Stop: the device is then set back into standby mode by the stop condition.

6 ELECTRICAL CHARACTERISTICS

6.1 Power-On Timing

The GD24CL256B has a built-in power-on-reset circuit that initializes itself at the same time during power-on. Unsuccessful initialization may cause a malfunction. To operate the power-on-reset circuit normally, the following conditions must be satisfied.

When initialization is successfully completed by the power-on-reset circuit, the GD24CL256B enters the standby status. tVSL is the time required to initialize the GD24CL256B. No instructions are accepted during this time.

Figure 13. Power-On Timing Sequence Diagram

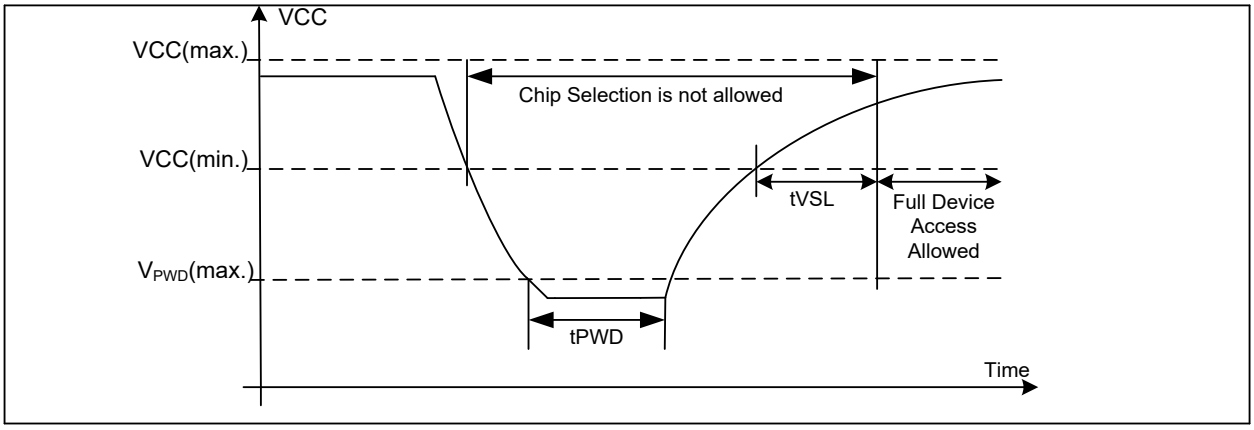


Table 7. Power-Up Timing and Write Inhibit Threshold

Symbol	Parameter	Min.	Max.	Unit
tVSL	VCC (min.) to device operation	20		μs
VWI	Write Inhibit Voltage		1.6	V
VPWD	VCC voltage needed to below VPWD for ensuring initialization will occur		0.6	V
tPWD	The minimum duration for ensuring initialization will occur	10		μs

6.2 Initial Delivery State

The device is delivered with the memory array all bits are set to 1 (each Byte contains FFH).

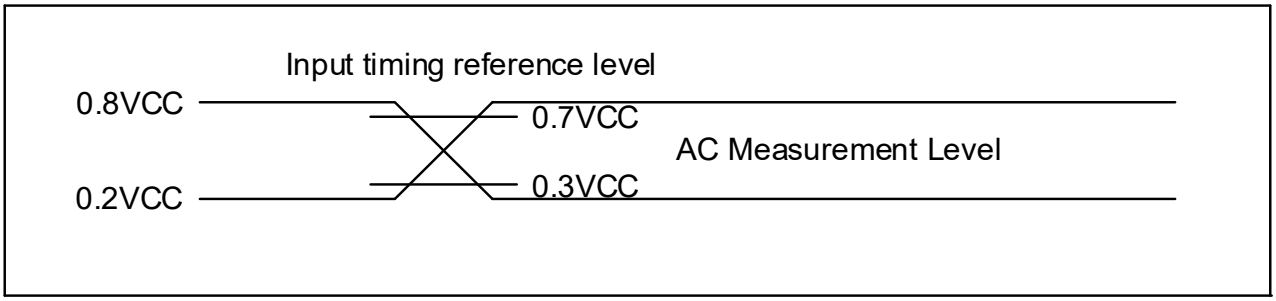
6.3 Absolute Maximum Ratings

Parameter	Value	Unit
Ambient Operating Temperature (TA)	-40 to 85	℃
Supply Voltage	-0.5 to 6.5	V
Voltage on Any Pin	-0.5 to 6.5	V
Temperature Under Bias	-55 to 125	℃
Storage Temperature	-65 to 150	℃
Output Current	5	mA

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

6.4 Capacitance

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance			6	pF	V_{IN}=0V
$C_{I/O}$	Input / Output Capacitance			8	pF	$V_{I/O}$=0V



6.5 DC Characteristics

(T_A = -40℃~85℃, VCC=1.7~5.5V)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit.
$C_{I/O}$	Input / Output Capacitance	$V_{I/O}$=0V				8	pF
C_{IN}	Input Capacitance	V_{IN}=0V				6	pF
I_{LI}	Input Leakage Current	V_{IN}=V_{CC}/V_{SS}				±2	μA
I_{LO}	Output Leakage Current	V_{OUT}= V_{CC}/V_{SS}				±2	μA
I_{CC1}	Standby Current	25℃	1.7V			1	μA
			2.5V			1	
			5.5V			1	
		85℃	1.7V			1	
			2.5V			1	
			5.5V			2	
		105℃	1.7V			2	
			2.5V			2	
			5.5V			3	
		125℃	1.7V			3	
			2.5V			3	
			5.5V			5	
I_{CC2}	Read Current	400KHz	1.7V			0.5	mA
			2.5V			1	
			5.5V			1	
		1MHz	1.7V			1	
			2.5V			1	
			5.5V			1	
I_{CC3}	Write Current	1.7V				1	mA
		2.5V				2	
		5.5V				3	
V_{IL}	Input Low Voltage			-0.5V		0.3VCC	V
V_{IH}	Input High Voltage			0.7VCC		VCC+1	V
V_{OL}	Output Low Voltage	VCC=1.7V, I_{OL}=1mA				0.2	V
		VCC=2.5V, I_{OL}=3.2mA				0.4	V

Note:

1. Typical value at TA = 25℃.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

6.6 AC Characteristics

(T_A = -40℃~125℃, VCC=1.7~5.5V)

Symbol	Parameter	1.7~5.5V		1.7~5.5V		1.7~5.5V		Unit.
		Min	Max.	Min	Max.	Min	Max.	
F_C	Clock Frequency		100		400		1000	KHz
t_{CLH}	Clock High Time	4000		600		260		ns
t_{CLL}	Clock Low Time	4700		1300		500		ns
t_{QHQL}	Output fall time		300		300		120	ns
t_R	Input signal rise time		1000	20	300	20	120	ns
t_F	Input signal fall time		300	20	300	20	120	ns
t_{DVCH}	Data In Setup Time	250		100		50		ns
t_{CLDX}	Data In Hold Time	0		0		0		ns
t_{CLQX}	Output Hold Time	50		50		50		ns
t_{CLQV}	Clock Low To Output Valid		3500	50	900	50	450	ns
t_{CHDL}	Start condition setup time	4700		600		250		ns
t_{DLCL}	Start condition hold time	4000		600		250		ns
t_{CHDH}	Stop condition setup time	4000		600		250		ns
t_{DHDL}/ t_{BUF}	Stop condition to next Start condition Latency	4700		1300		500		ns
t_{NS}	Noise Pulse Filtered at SCL and SDA Inputs		50		50		50	ns
t_{WLDL}	WP setup time (before the Start condition)	0		0		0		μs
t_{DHWH}	WP hold time (after the Stop condition)	2.5		2.5		1		μs
t_W	Internal Write cycle duration		5		5		5	ms

Note:

1. Typical value at T_A = 25℃.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

Figure 14. Input Timing

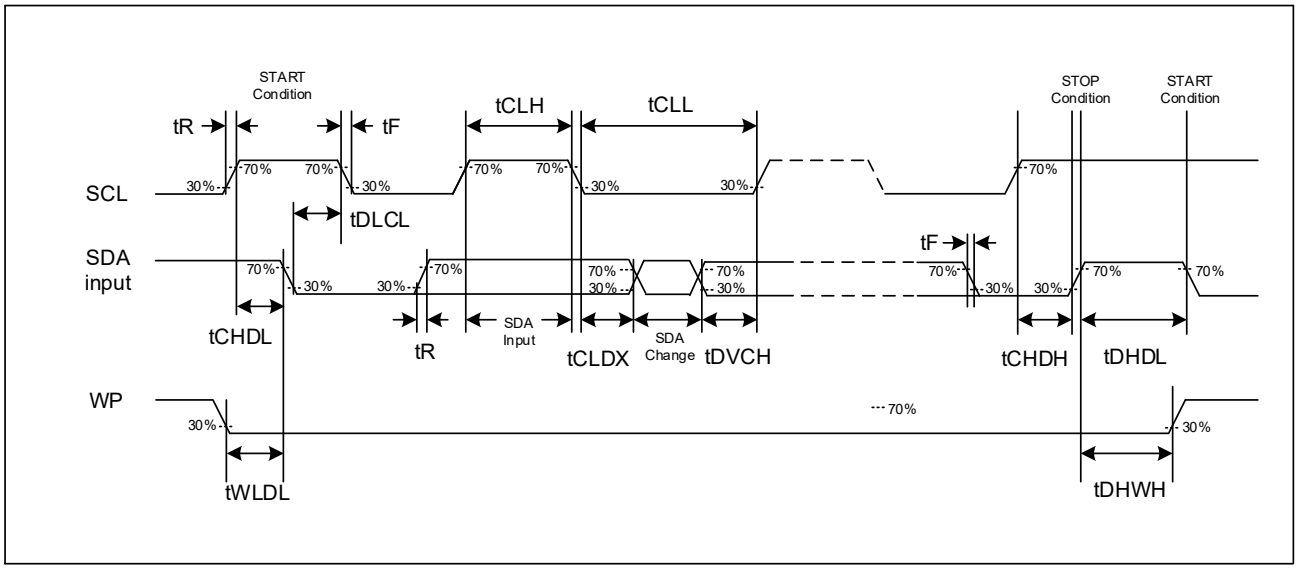
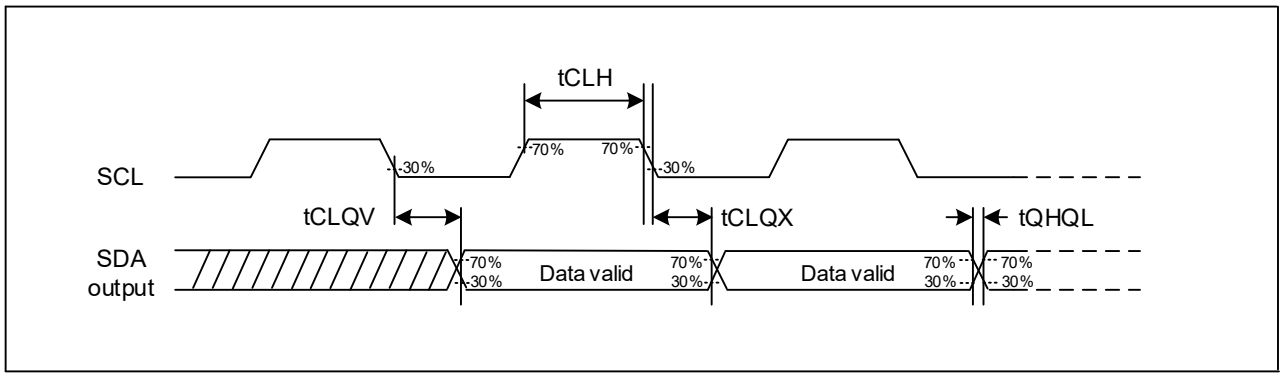
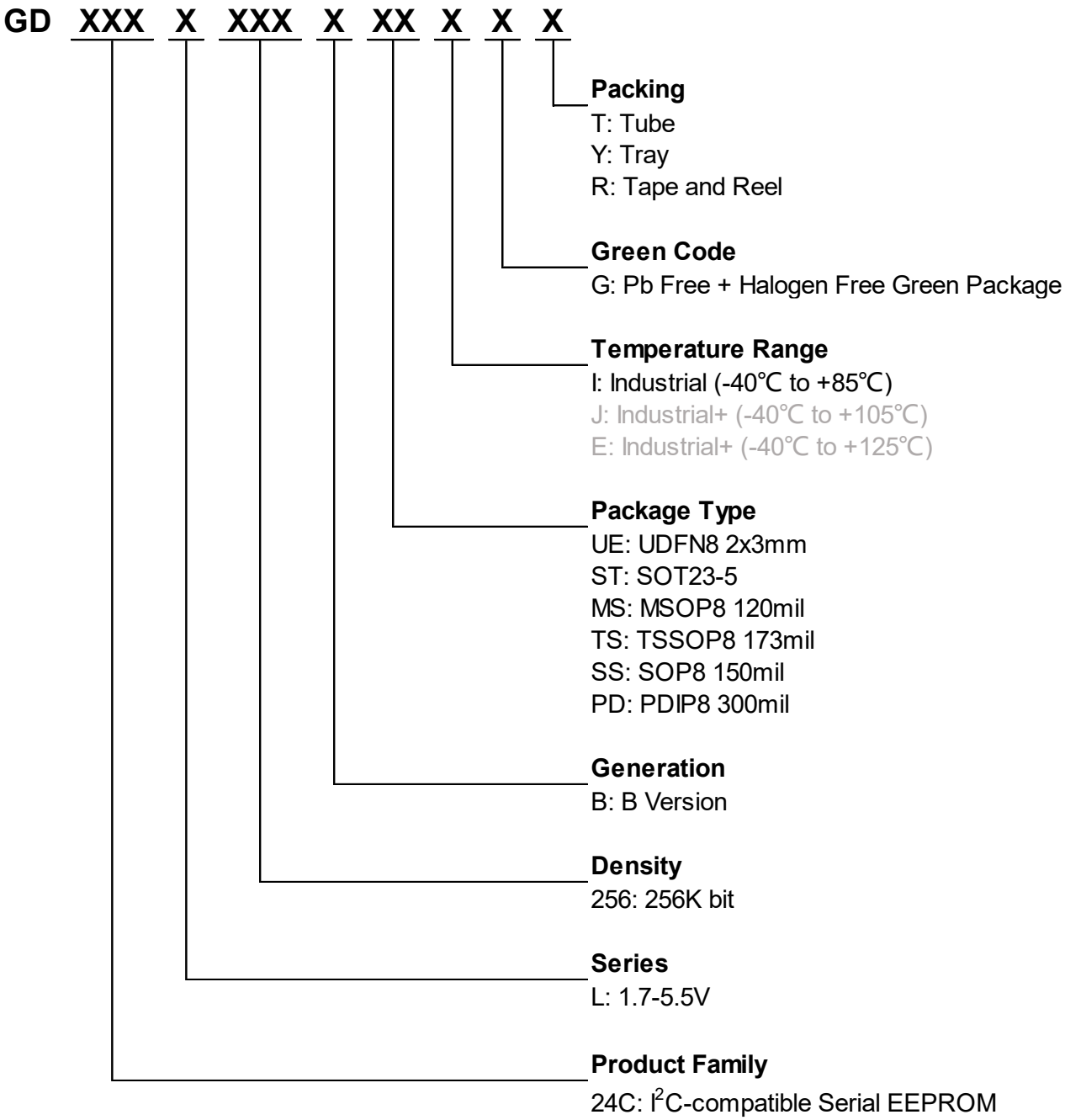


Figure 15. Output Timing



7 ORDERING INFORMATION



7.1 Valid Part Numbers

Please contact GigaDevice regional sales for the latest product selection and available form factors.

Temperature Range I: Industrial (-40℃ to +85℃)

Product Number	Density	Package Type	Packing Options
GD24CL256BUEIG	256Kbit	UDFN8 2x3mm	R
GD24CL256BSTIG	256Kbit	SOT23-5	R
GD24CL256BMSIG	256Kbit	MSOP8 120mil	R
GD24CL256BTSIG	256Kbit	TSSOP8 173mil	R
GD24CL256BSSIG	256Kbit	SOP8 150mil	T/Y/R
GD24CL256BPDIG	256Kbit	PDIP8 300mil	T

Temperature Range J: Industrial+ (-40℃ to +105℃)

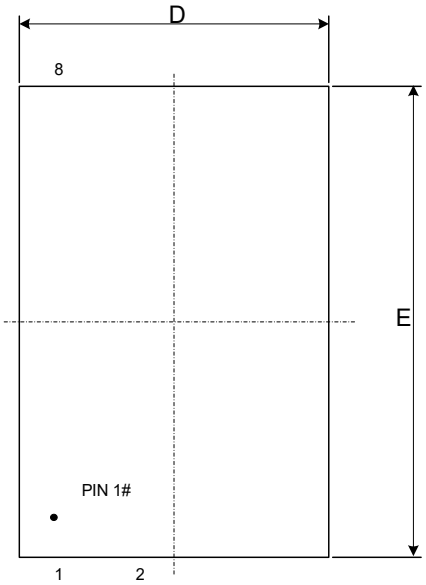
Product Number	Density	Package Type	Packing Options
GD24CL256BUEJG	256Kbit	UDFN8 2x3mm	R
GD24CL256BSTJG	256Kbit	SOT23-5	R
GD24CL256BMSJG	256Kbit	MSOP8 120mil	R
GD24CL256BTSJG	256Kbit	TSSOP8 173mil	R
GD24CL256BSSJG	256Kbit	SOP8 150mil	T/Y/R
GD24CL256BPDJG	256Kbit	PDIP8 300mil	T

Temperature Range E: Industrial+ (-40℃ to +125℃)

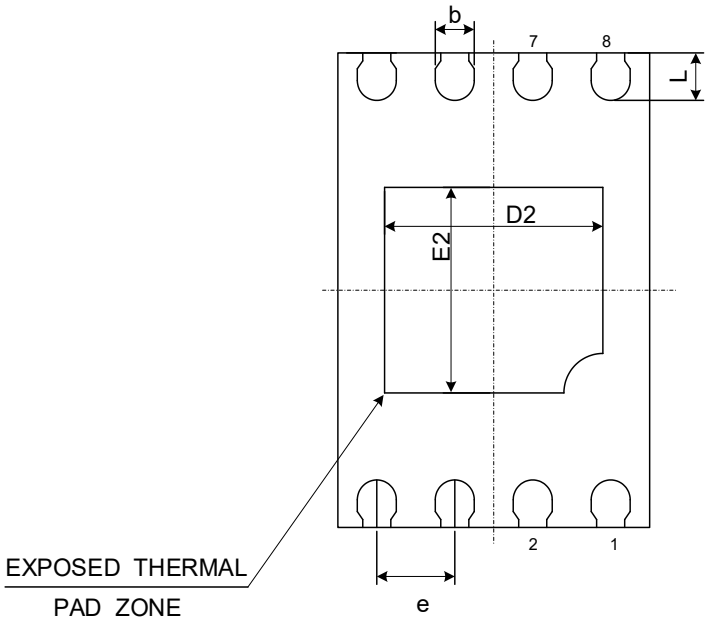
Product Number	Density	Package Type	Packing Options
GD24CL256BUEEG	256Kbit	UDFN8 2x3mm	R
GD24CL256BSTEG	256Kbit	SOT23-5	R
GD24CL256BMSEG	256Kbit	MSOP8 120mil	R
GD24CL256BTSEG	256Kbit	TSSOP8 173mil	R
GD24CL256BSSEG	256Kbit	SOP8 150mil	T/Y/R
GD24CL256BPDEG	256Kbit	PDIP8 300mil	T

8 PACKAGE INFORMATION

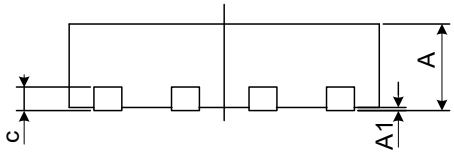
8.1 Package UDFN8 (2x3mm)



Top View



Bottom View



Side View

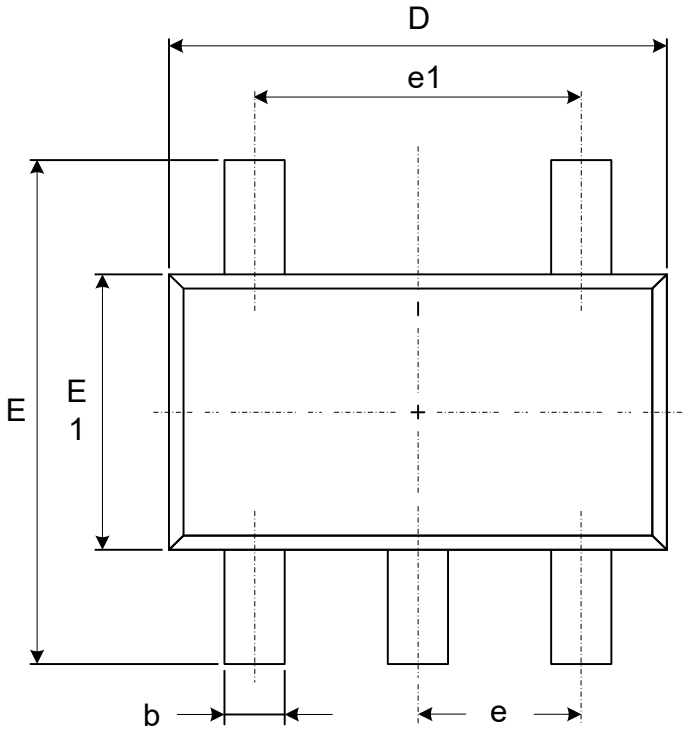
Dimensions

Symbol / Unit		A	A1	c	b	D	D2	E	E2	e	L
mm	Min	0.50	0.00	-	0.18	1.90	1.25	2.90	1.15	0.50 BSC	0.20
	Nom	0.55	0.02	0.152 REF	0.25	2.00	1.40	3.00	1.30		0.30
	Max	0.60	0.05	-	0.30	2.10	1.50	3.10	1.40		0.40

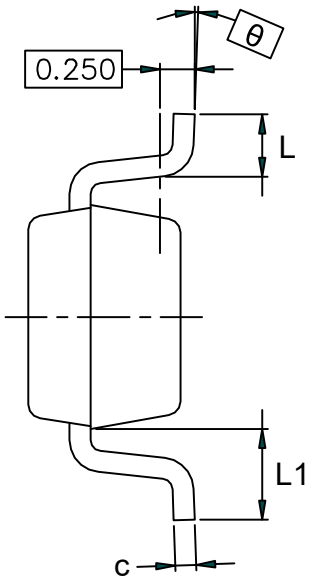
Note:

1. The lead shape and e-PAD notch may be of little difference according to different package factories. These lead shapes are compatible with each other.
2. Coplanarity ≤0.08mm.

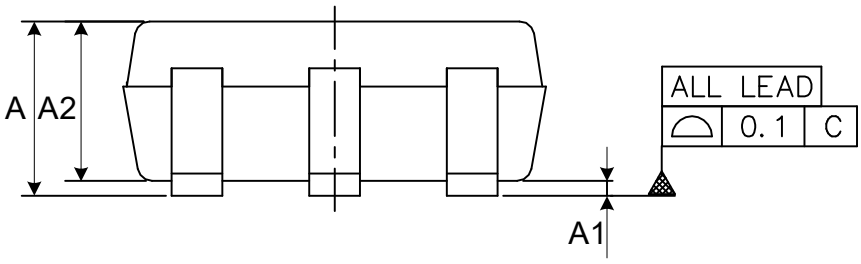
8.2 Package SOT23-5



Top View



Side View

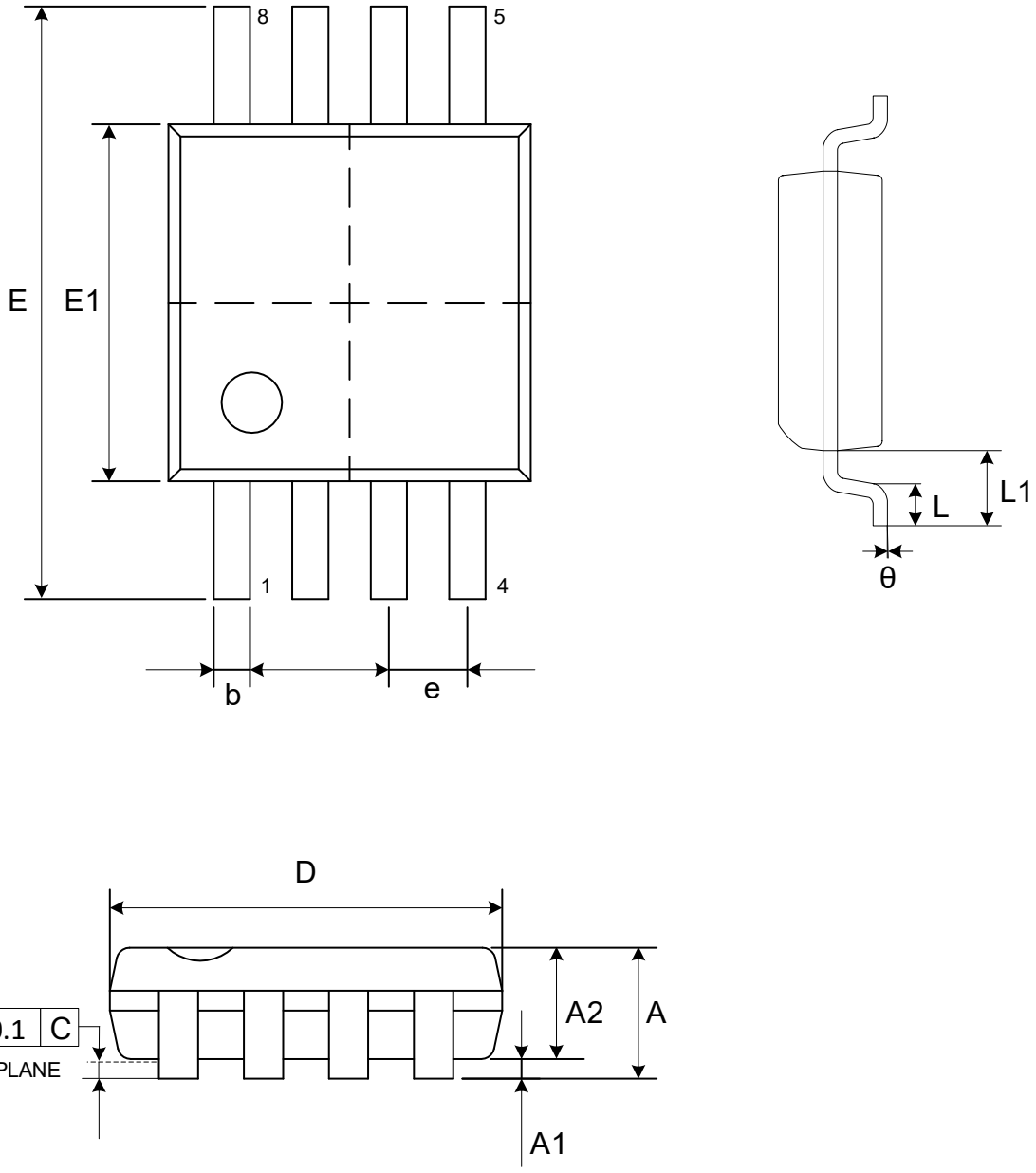


Front View

Dimensions

Symbol / Unit		A	A1	A2	B	c	D	E	E1	e	e1	L	L1	θ
mm	Min	-	0.04	1.00	0.30	0.13	2.82	2.60	1.50	0.95	1.90	0.30	0.60	0°
	Nom	-	-	1.10	-	-	2.92	2.80	1.60			-		-
	Max	1.250	0.10	1.20	0.45	0.23	3.02	3.00	1.70			0.60		8°

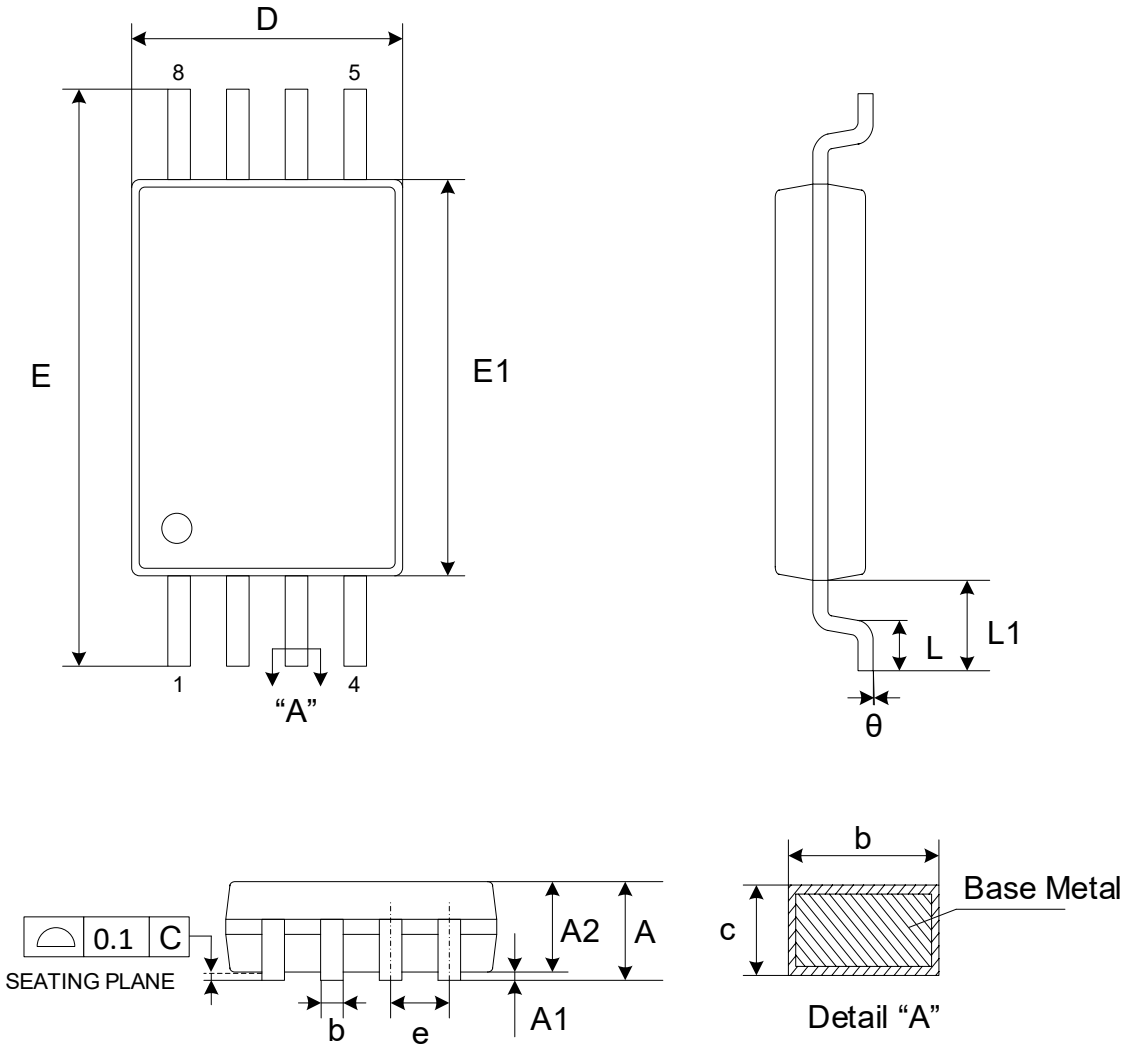
8.3 Package MSOP8 120MIL



Dimensions

Symbol / Unit		A	A1	A2	b	c	D	E	E1	e	L	L1	θ
mm	Min	-	0.00	0.75	0.28	0.15	2.90	4.70	2.90	0.650	0.45	0.95	0°
	Nom	-	-	0.85	-	-	3.00	4.90	3.00		-		-
	Max	1.10	0.15	0.95	0.35	0.23	3.10	5.10	3.10		0.75		8°

8.4 Package TSSOP8 173MIL



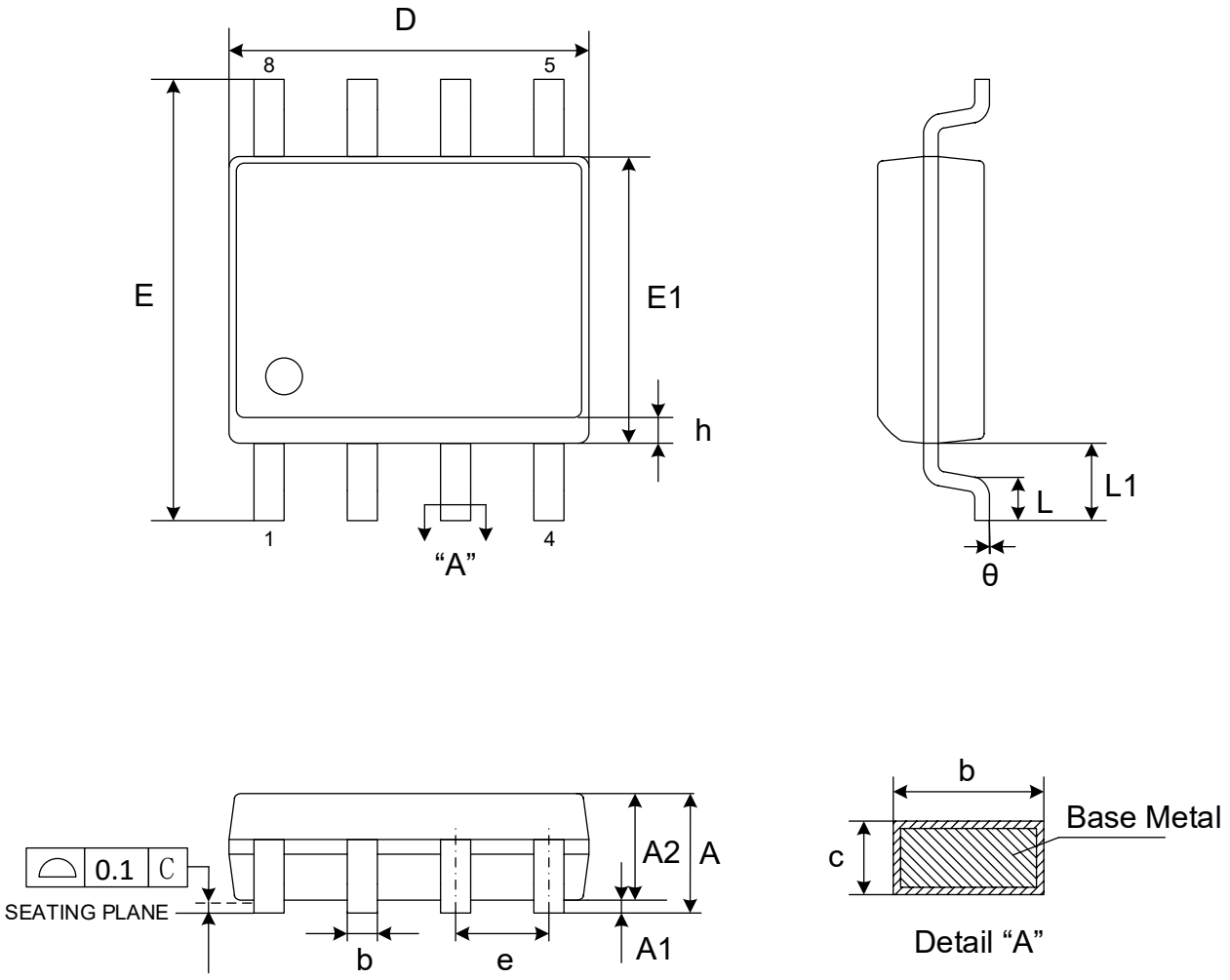
Dimensions

Symbol / Unit		A	A1	A2	b	c	D	E	E1	e	L	L1	θ
mm	Min	-	0.05	0.80	0.19	0.09	2.90	6.20	4.30	0.65	0.45	1.00	0°
	Nom	-	0.10	1.00	0.25	0.15	3.00	6.40	4.40		-		-
	Max	1.20	0.15	1.05	0.30	0.20	3.10	6.60	4.50		0.75		8°

Notes:

1. Both package length and width do not include mold flash.

8.5 Package SOP8 150MIL



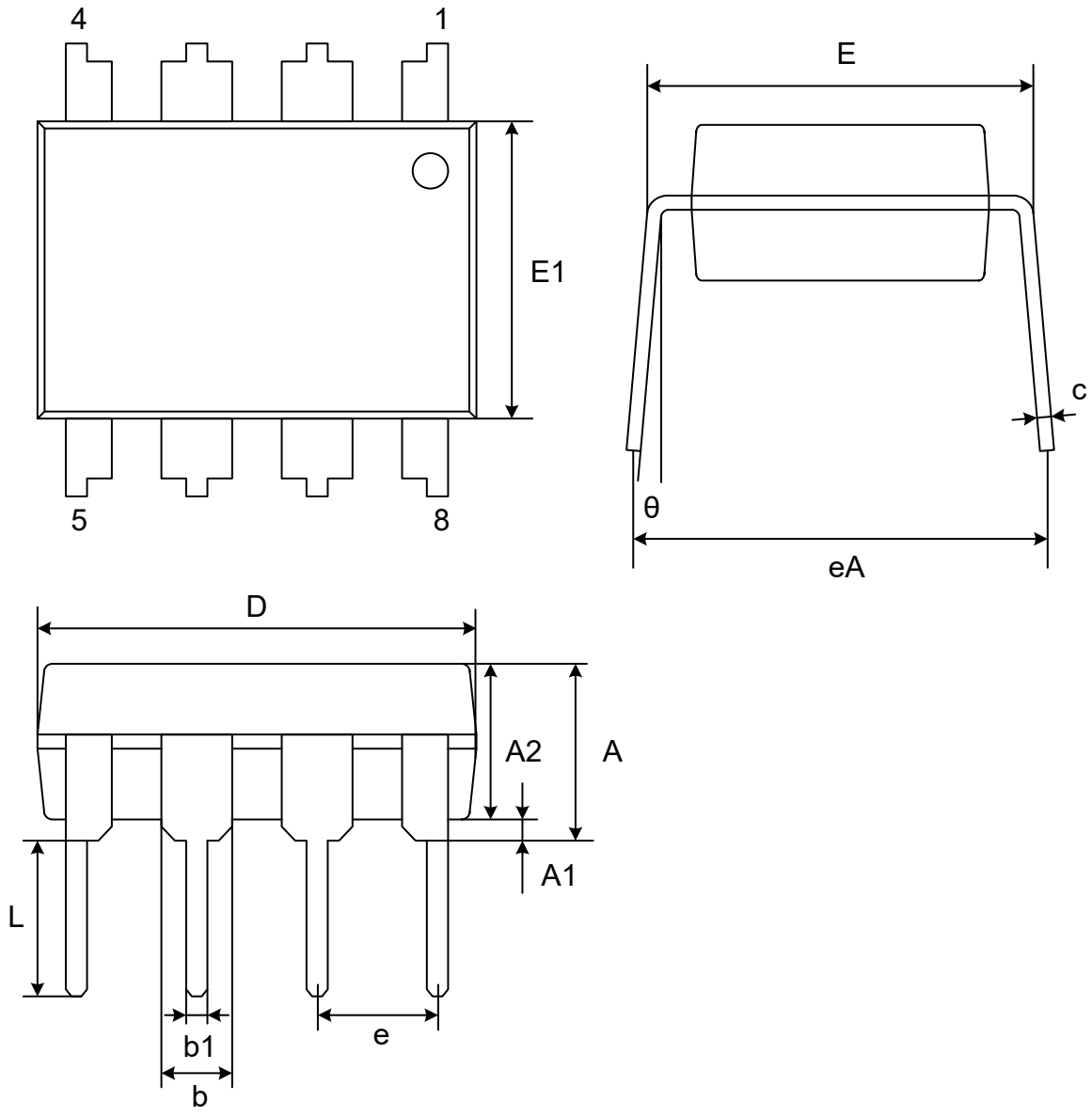
Dimensions

Symbol / Unit		A	A1	A2	b	c	D	E	E1	e	L	L1	h	θ
mm	Min	-	0.10	1.25	0.31	0.10	4.80	5.80	3.80	1.27	0.40	1.04	0.25	0°
	Nom	-	0.15	1.45	0.41	0.20	4.90	6.00	3.90		-		-	-
	Max	1.75	0.25	1.55	0.51	0.25	5.00	6.20	4.00		0.90		0.50	8°

Note:

1. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per end.
2. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per end.

8.6 Package DIP8 300MIL



Dimensions

Symbol / Unit		A	A1	A2	b	b1	C	D	E	E1	e	L	eA	θ
mm	Min	-	0.38	3.00	1.14	0.36	0.20	9.02	7.62	6.10	2.54	2.92	8.45	0°
	Nom	-	-	3.30	1.52	0.46	0.25	9.27	7.87	6.35		3.30	8.90	-
	Max	3.88	-	3.50	1.78	0.56	0.35	9.59	8.26	6.60		3.81	9.35	11°

Note: Both the package length and width do not include the mold flash.

9 REVISION HISTORY

Version No	Description	Page	Date
0.1	Preliminary release	All	2024-10-25
0.2	Modify “Additional security page” -> “Additional write lockable security page” Add note for SOT23-5 package Update description of device addressing Update AC parameter temperature range to -40℃~125℃ Update Dimensions of UDFN8 2x3mm	P4 P6 P12 P20 P24	2025-4-10
0.3	Update VIH(max) to VCC+1V Update Input/Output Timing	P19 P21	2026-4-23

Preliminary Designation

The “Preliminary” designation on a GigaDevice datasheet indicates that the product is not fully characterized. The specifications are subject to change and are not guaranteed. GigaDevice or an authorized sales representative should be consulted for current information before using this product.

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